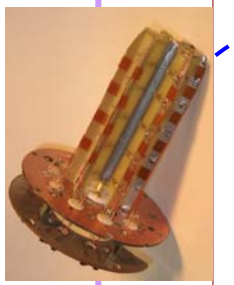
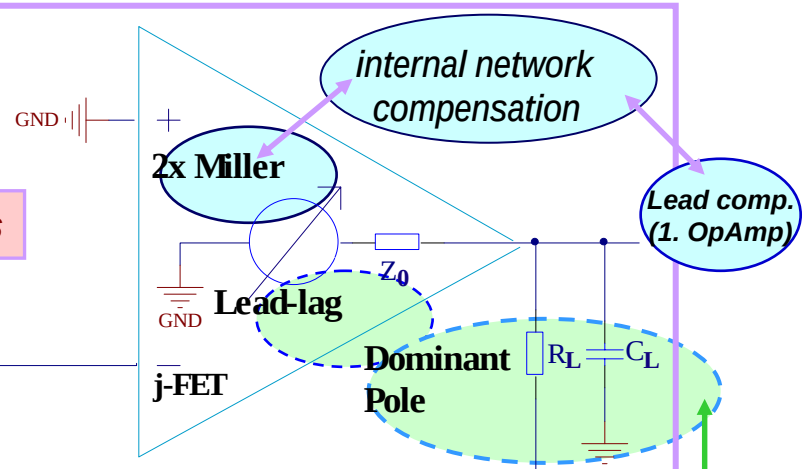
AGATA Core - upgraded front end electronics

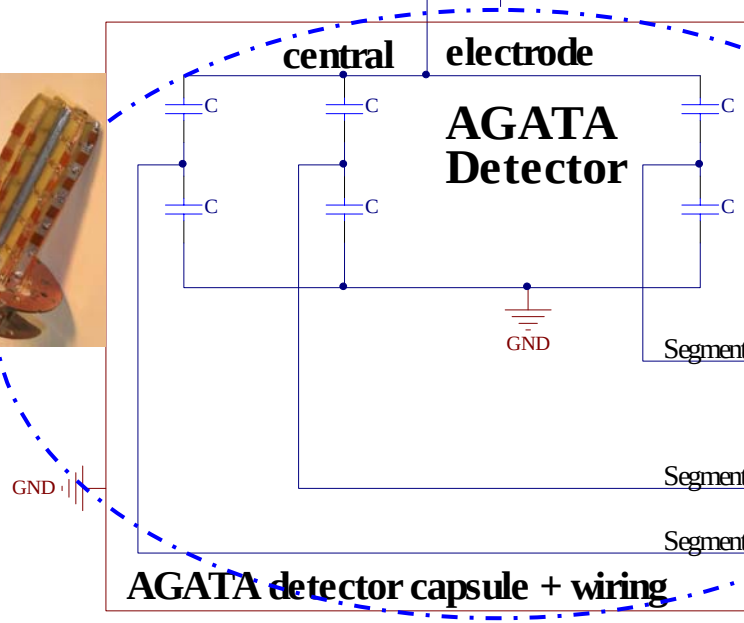
- *Upgraded Charge Sensitive Preamplifier*
  - *extended frequency compensation from Single Gain implemented also in the Dual Gain Core as presented at Uppsala, July, 2008*
- *Reworked Dual Gain Core ⇔ **fully** reconfigurable*
  - ***either Single or Dual***
  - ***either LV-CMOS or LVDS***
  - ***full production of first series of 20 pcs. & tested***
- *Programmable Spectroscopic Pulser ⇔ unchanged*

AGATA Single & Dual Gain Core reworked frequency compensations

Cryostat wiring as part of the front-end electronics

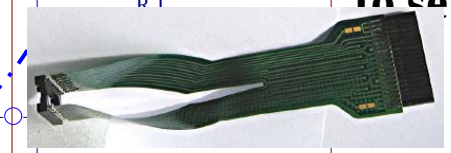






- *minimum Miller effect* (min.)
- *lead compensation* (min.)
- *lead-lag compensation* (adj.)
- *dominant pole compensation* (adj.)

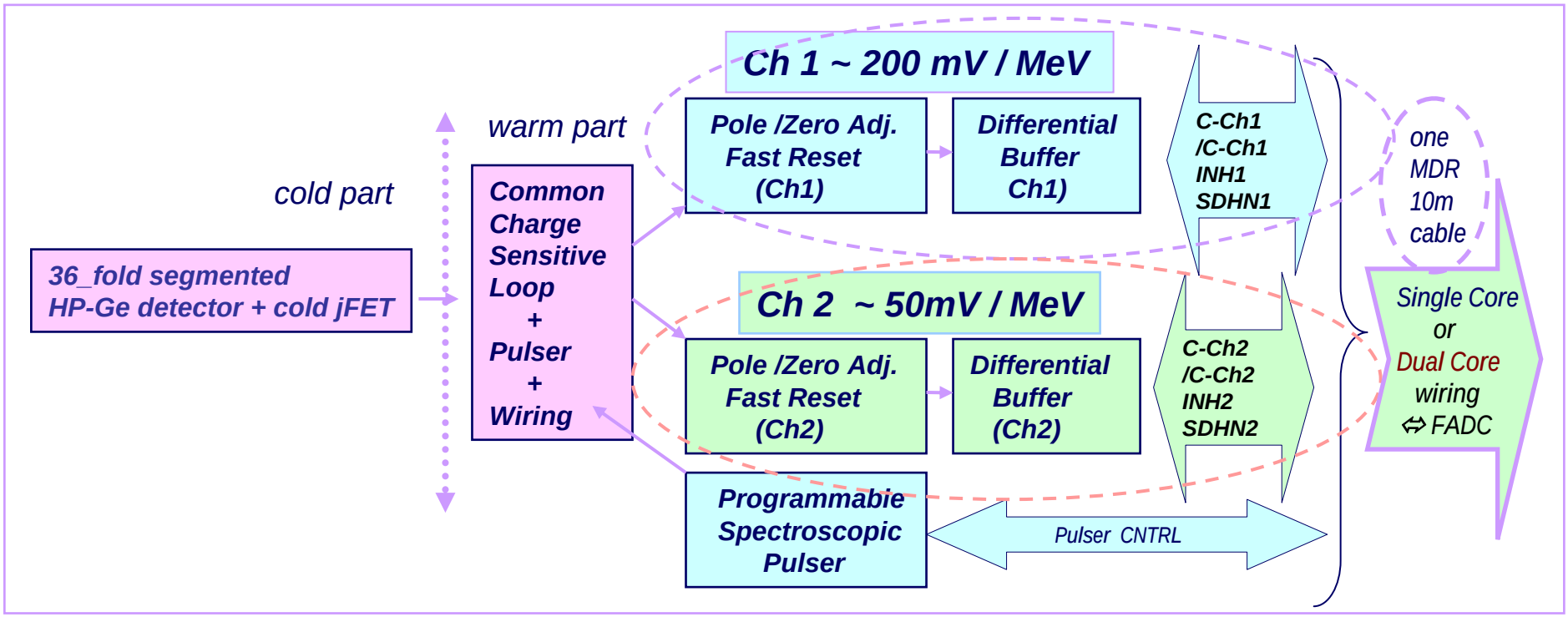
external network compensation

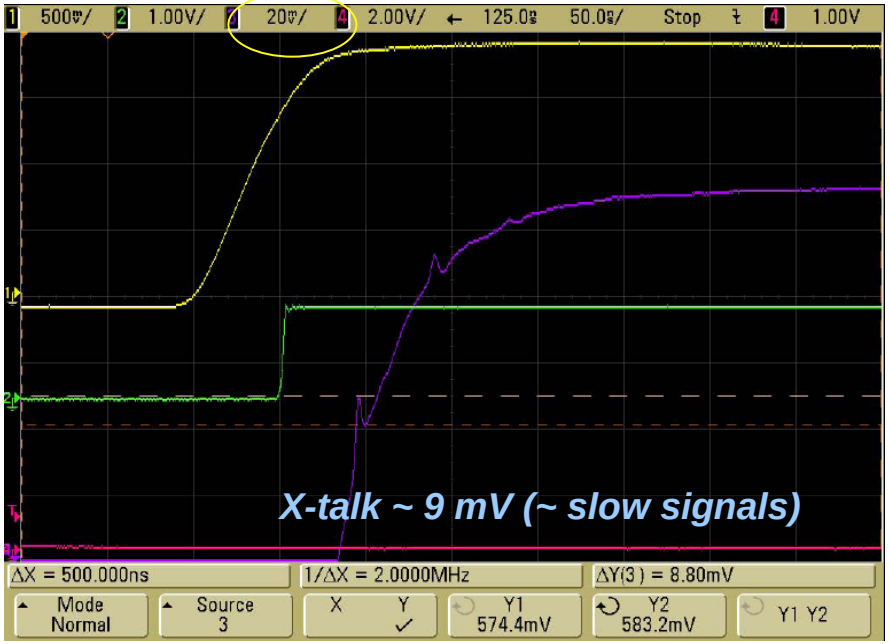


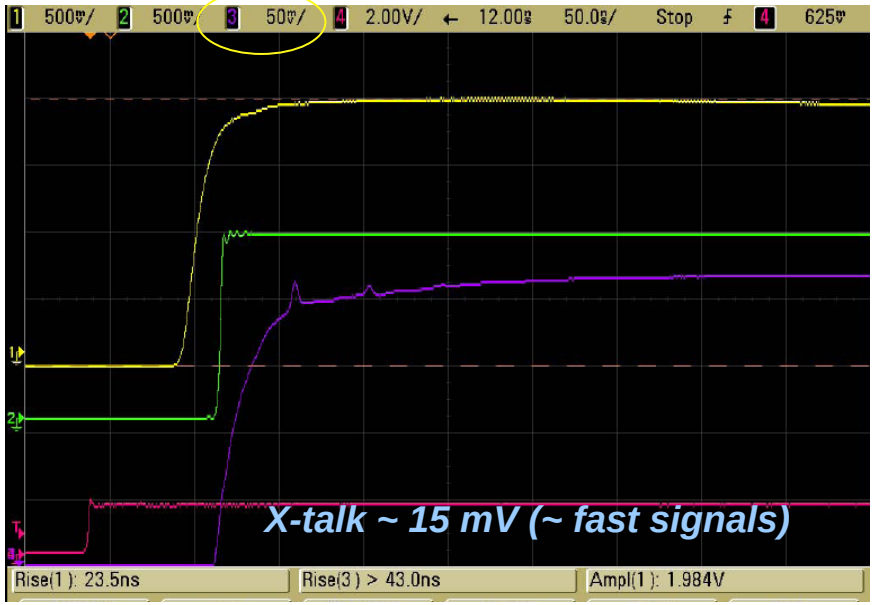
to segment preamplifiers

Dual Gain Core - the upgraded features and its structure

- *Linear Range: 2keV -180 MeV (far beyond the ADC limit ~100dB !)*
- *Two modes of operations, four ranges:*
  - *a) Pulse Amplitude (0-5 MeV); (0-20 MeV)* ⇔ *b) Time Over Threshold (ToT) (5-180 MeV); (20-180 MeV)*







Issue: ***INH-C1 and Core Ch2 X-talk on the transmission line due to INH-C1 return GND …***

a) keeping INH-C as LV-CMOS digital signal

Advantage:

- simple upgrade of the single gain core to dual gain core

Disadvantage:

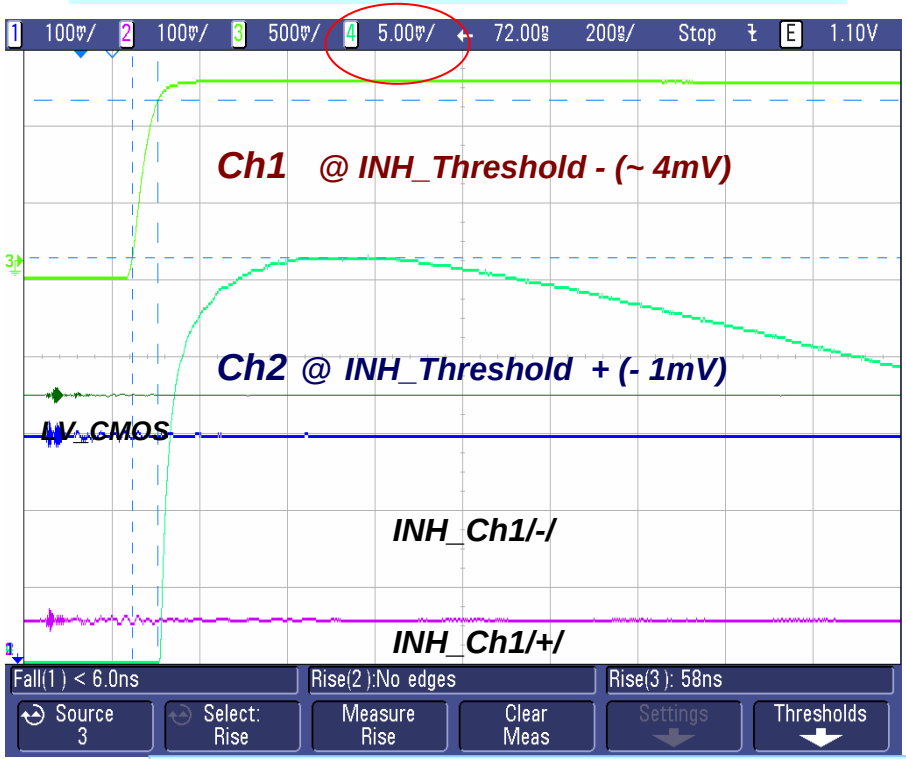
- relative large crosstalk ⇔ INH-C1 and 2.nd core signal

INH-C1 ⇔ Core_Ch2 (analog)

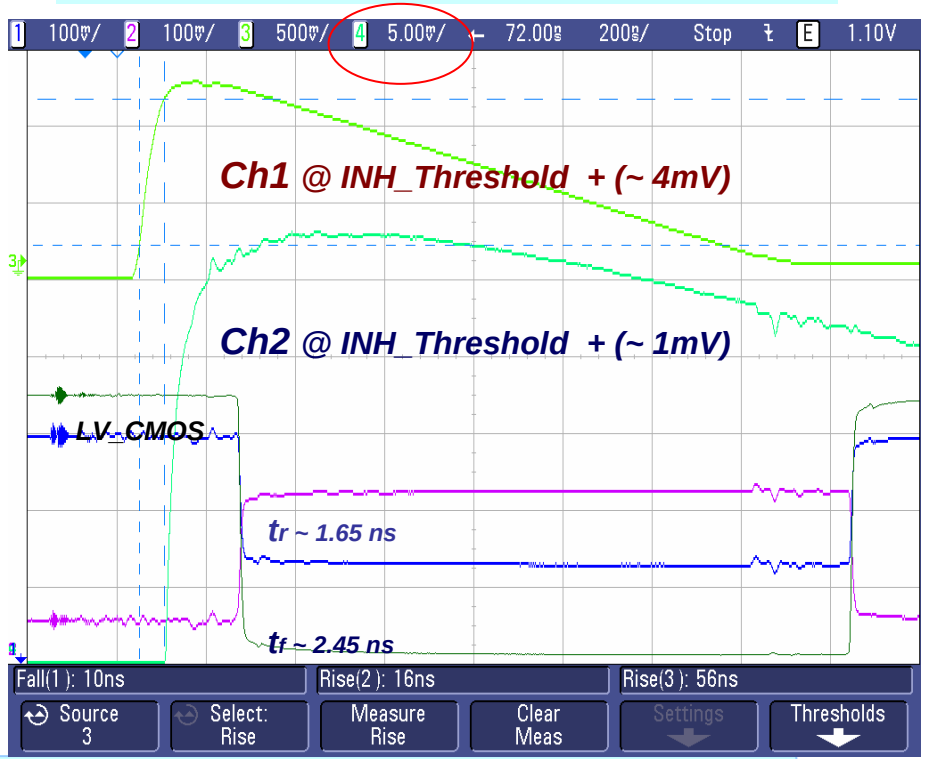
AGATA Dual_Core LVDS transmission of digital INH and Pulser_In signals

Solution: *AGATA Dual Core crosstalk test measurements*
Ch2 (analog signal) vs. LVDS-INH-C1 (bellow & above threshold)

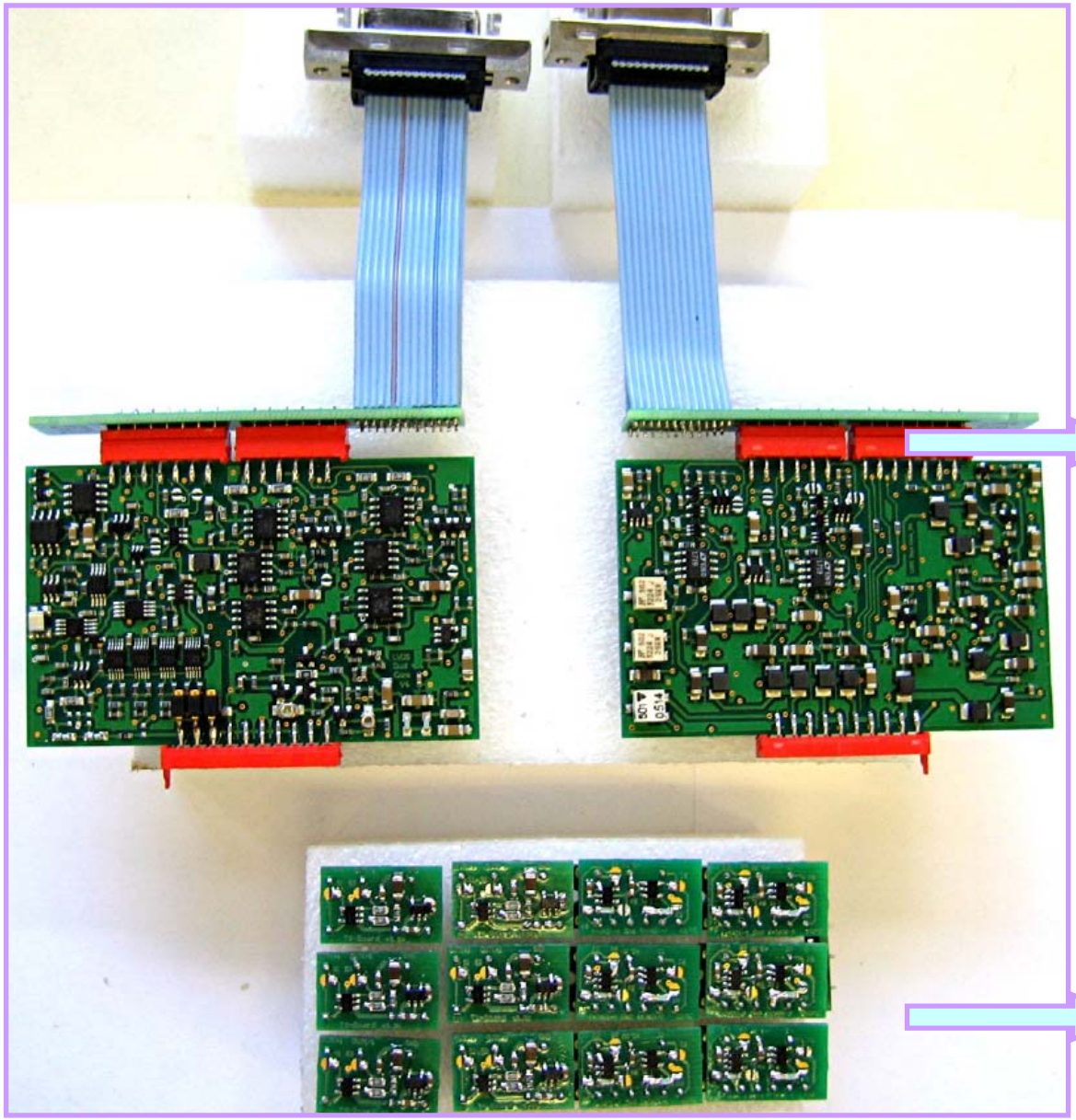
Core amplitude just below the INH threshold



Core amplitude just above the INH threshold



(1) Core_Ch1, (2) Core_Ch2, (3) INH_Ch1(LVDS/-/, (4) INH_Ch1(LVDS/+/)



User reconfigurable AGATA Dual Core

-***Dual gain core*** ***with:***

- ***5MeV and 20 MeV range***
- ***LV-DS or LV-CMOS digital handshaking signals***

-***Single gain core*** ***with either***

- ***5MeV or 20 MeV range***

⇔ including floating motherboard with flat band cable and MDR connector

AGATA FADC

tiny converter boards CMOS⇔LVDS

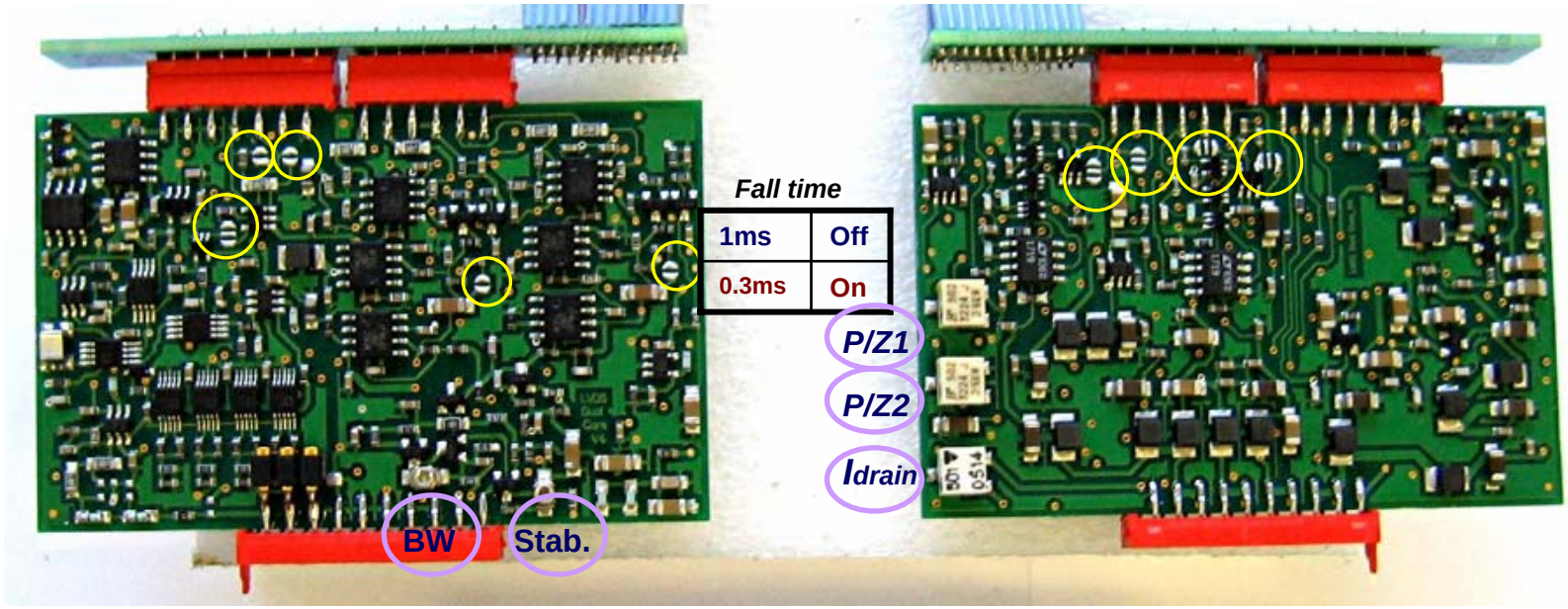
-NB: - originally, in FADC the core channel structure is with two gains, but only one input and LV-CMOS as I/O handshaking signals

- New: -to convert this structure into dual gain core with two inputs and either LV-DS or LV-CMOS digital signals for the INH-C1, INH-C2 and Pulser Trigger

Reconfigurable Dual Gain Core - *solderable converter switches from / to LV-DS ⇔ LV-CMOS*

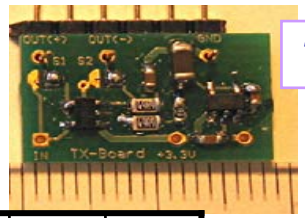
CMOS	Up	On	Off
LVDS	Down	Off	On

CMOS	Up	Down	Left	Right
LVDS	Down	Up	Right	Left



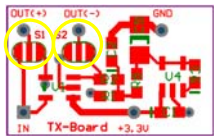
Fall time	
1ms	Off
0.3ms	On

FADC tiny converter boards from / to LV-DS ⇔ LV-CMOS



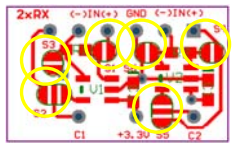
TX + 1.2V(Com)

CMOS	Left	Left
LVDS	Right	Right



Pulser Trigger

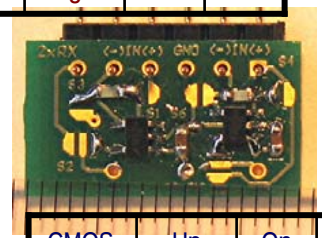
2 x RX



INH_C1 & INH-C2

CMOS	Left	On	Off
LVDS	Right	Off	On

INH-C1



CMOS	Up	On	Off
LVDS	Down	Off	On

INH-C2

Dual Gain Core - the upgraded features and its structure

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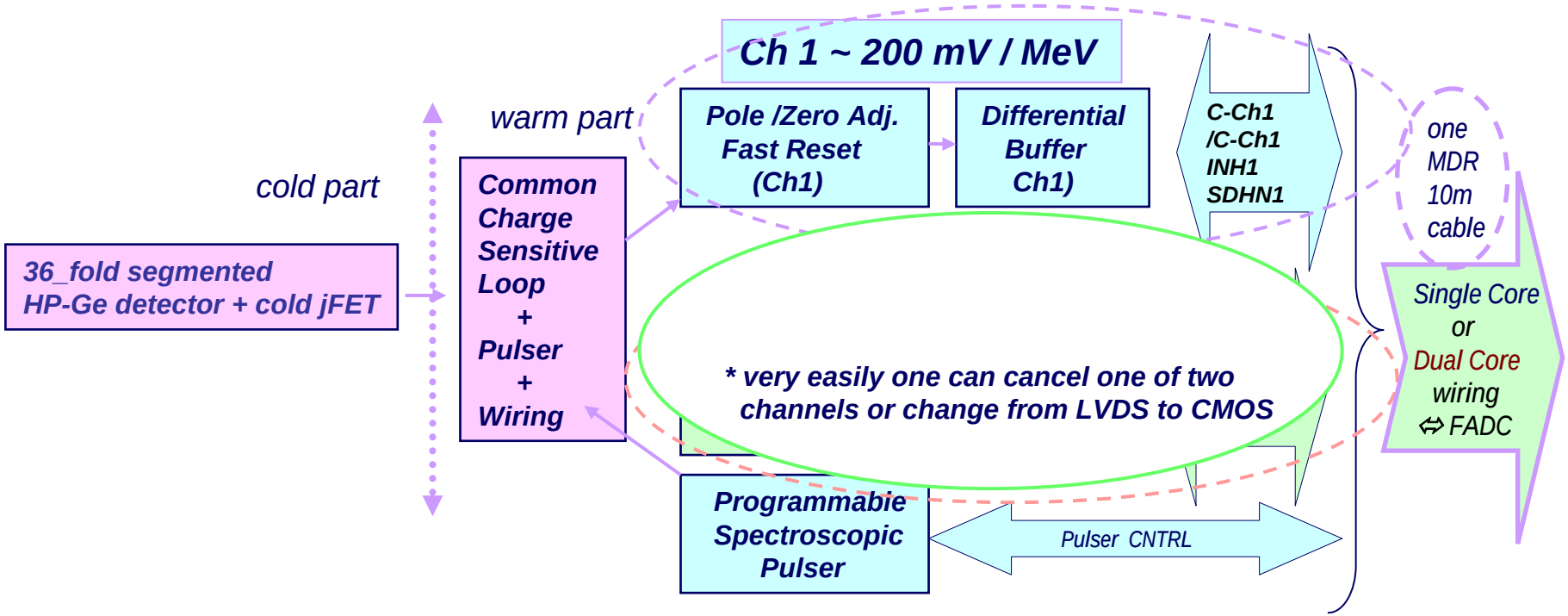

Conclusions

- *the conversion range has been successfully extended by more than one order of magnitude with the new spectroscopic ToT technique:*
  - *two modes of operation and four sub-ranges, namely:*
  - *0 ⇔ 5 (20) MeV and 5(20) ⇔ 180 MeV*
- *the use of the LV-DS signals (INH-C1, INH-C2 and Pulser Trigger) in the AGATA Dual Gain Core reduced considerable the crosstalk in the transmission line*
- *20 x sets for AGATA Reconfigurable Core manufactured, tested, ready to be used*
  - *(* each set consists of warm preamplifier, MDR-flat cable subassembly and FADC converter boards)*