

GTS Status

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on behalf of GTS working group

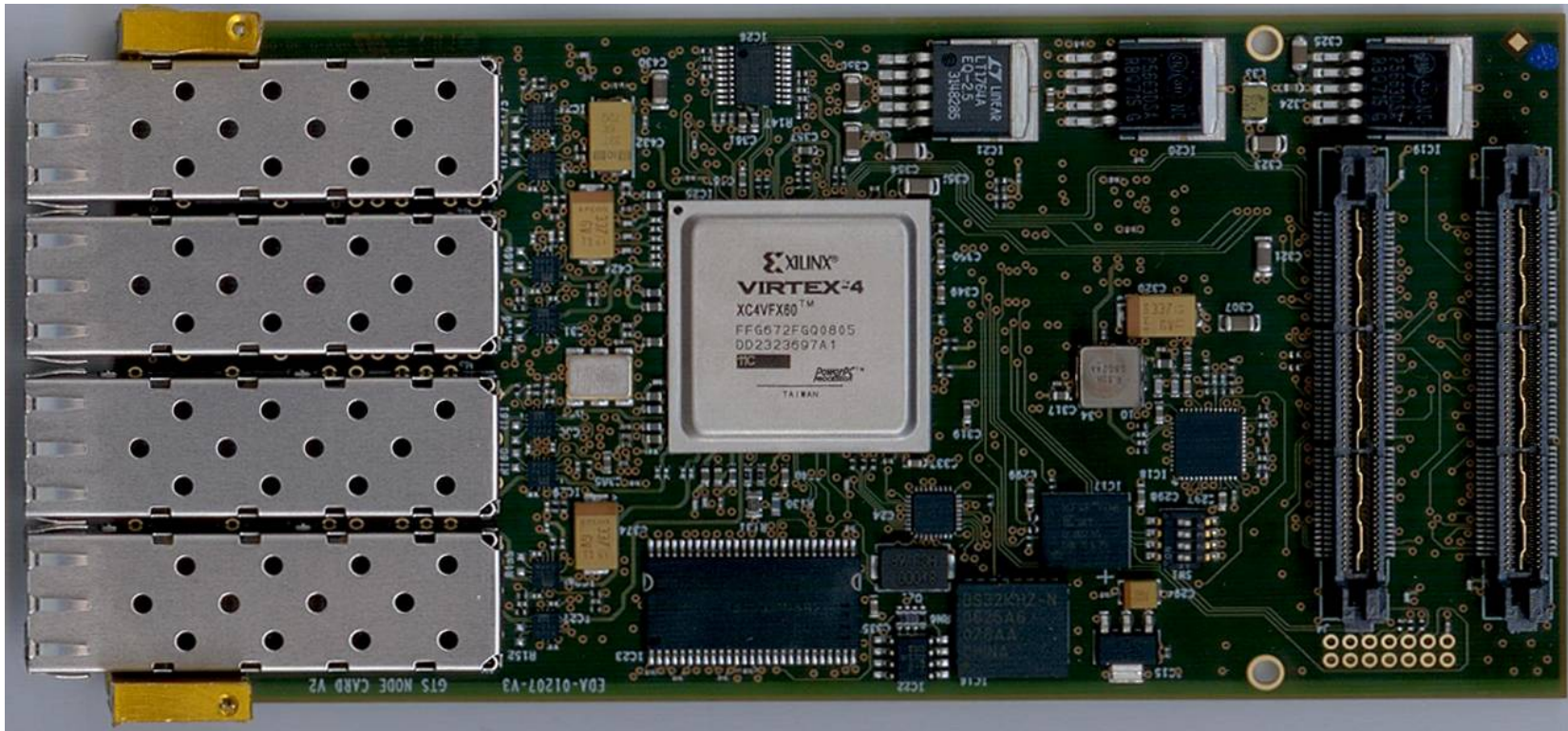
GTS @ the AGATA Demonstrator

- Mini tree (1 root – 3 destinations) based on mezzanines in deployment since Oct 2008
- (Almost) Fully functional
 - Includes automated tree discovery
 - Automated alignment
 - Basic slow control
 - Triggerless operation
 - Root node validates all trigger requests
- **Stable operation**

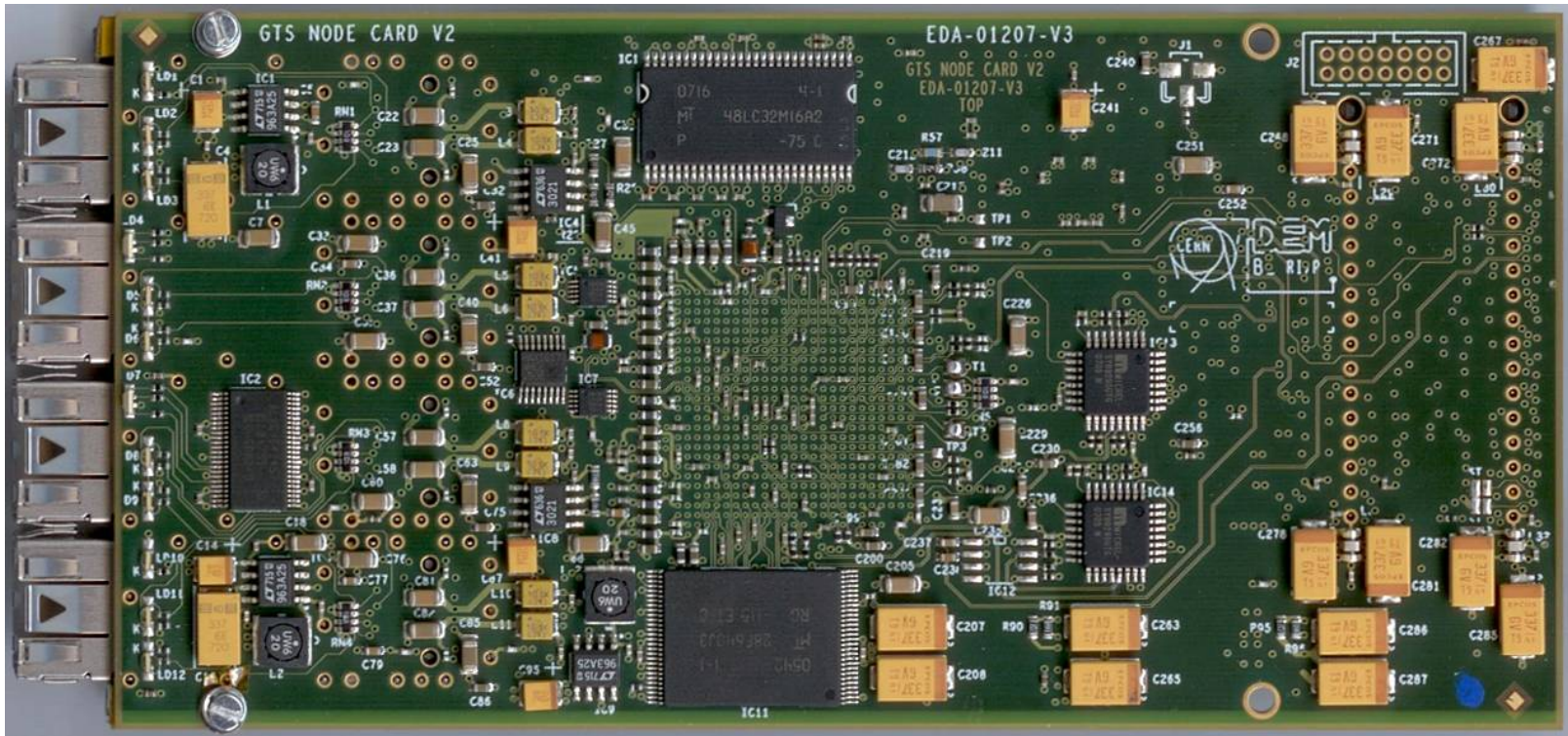
Revised GTS Mezzanine

- Improved clocking scheme
 - 100 MHz, 200 MHz, 250 MHz clock available
 - 250 MHz for 2.5Gb/s connection with GTP
- New PLL (same as in the carrier)
 - Smaller footprint
 - Better jitter filtering
 - Lower cost than former device (Vectron FX-200)

Revised GTS Mez. - prototype



Revised GTS Mez. - prototype

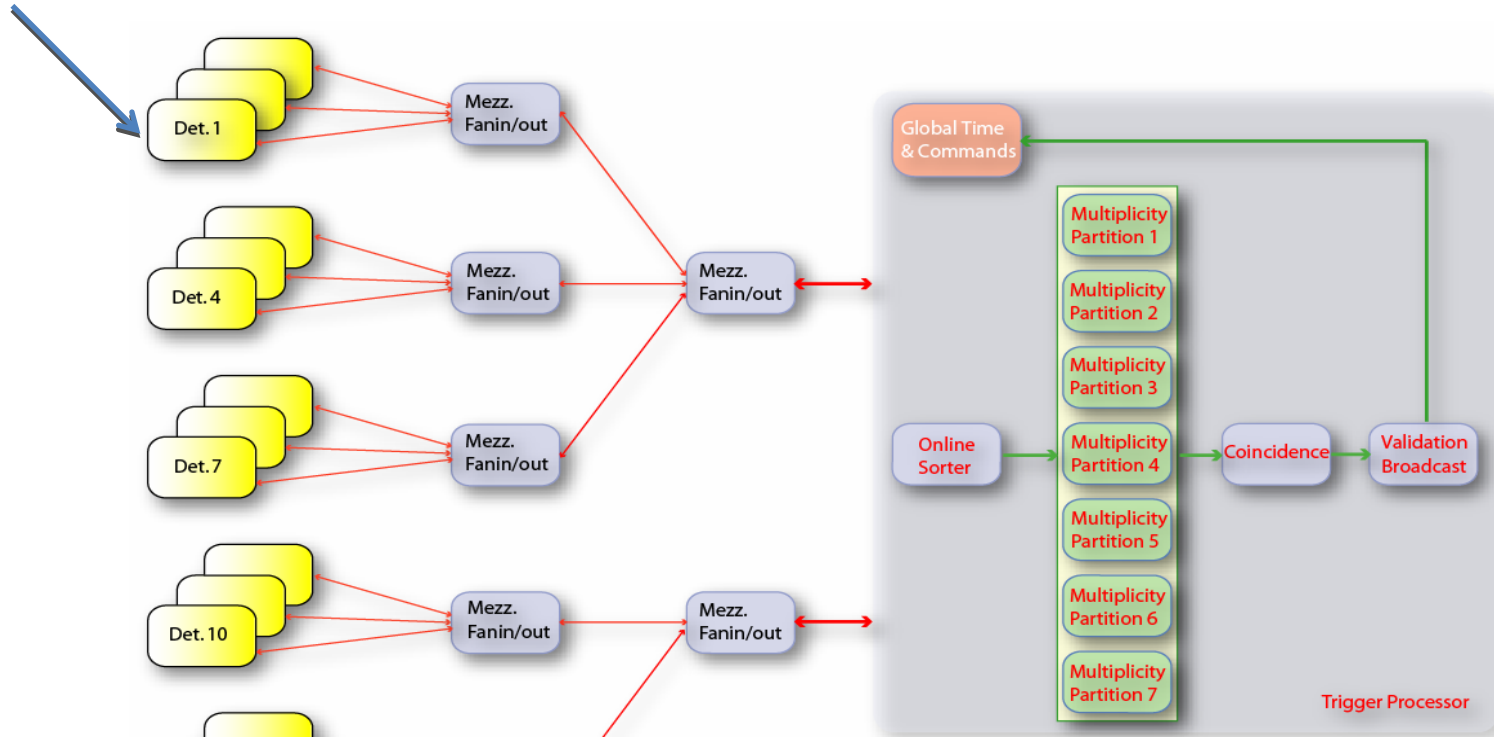


Revised GTS Mezzanine - status

- Two prototypes mounted
 - We are in the critical path !
- Being tested in Padova now
- Qualification in the demonstrator follows
 - April 09
- Phased production of
 - 10 units in may/june 09
 - 20 units in Q4

Global Trigger Processor

Max 1 MHz trigger requests/channel



48 channels in a Xilinx Virtex-4 Fx100

Agata Week - Cologne - March 2009



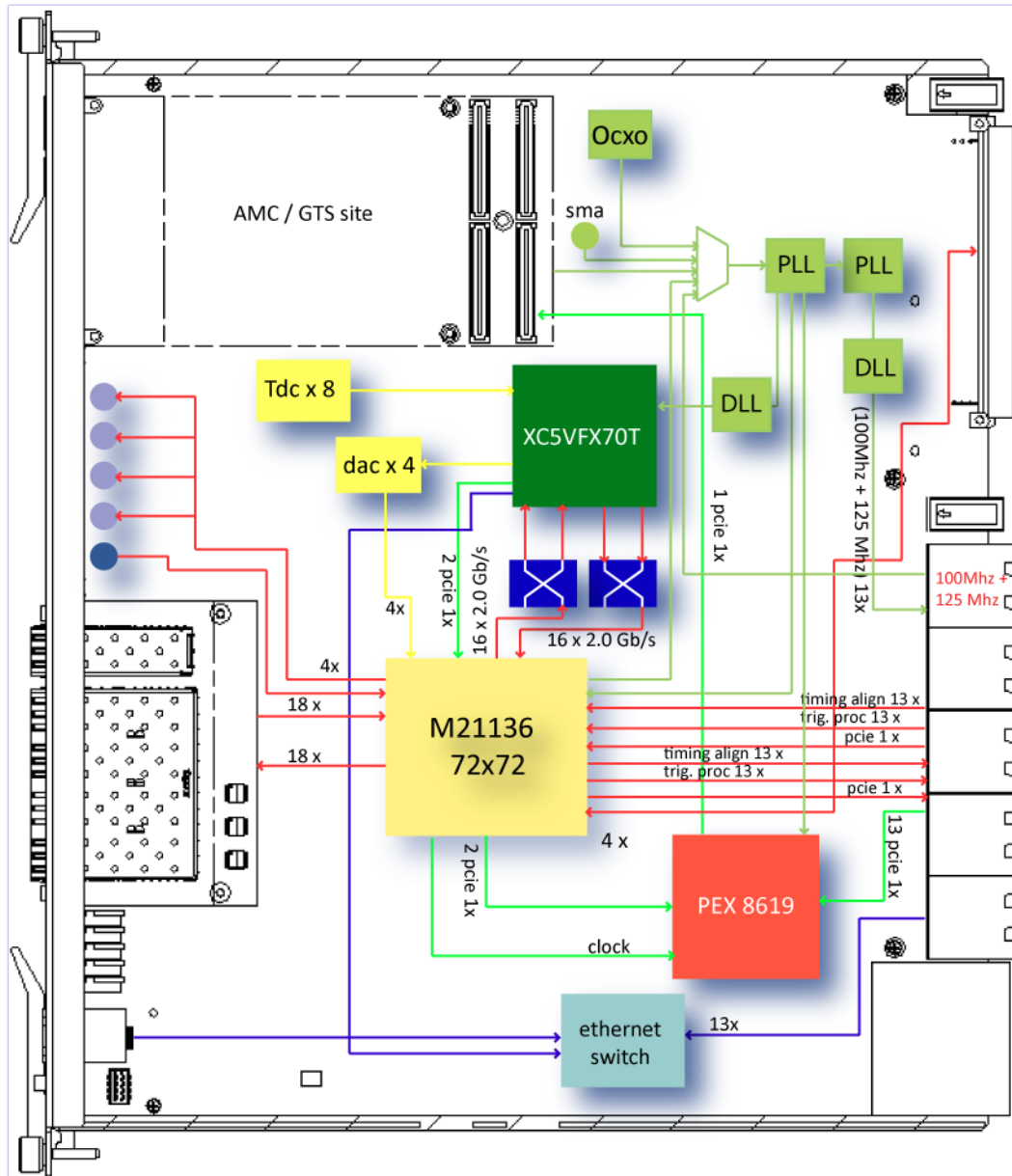
Global Trigger Processor

- Standalone unit
 - Completely general purpose
 - Only one fiber connection with root node
 - Manages 48 Agata crystal/ancillary channels
 - Place & Routed in 85% of a Xilinx Virtex4-FX100
- Being integrated in the demonstrator chain
 - Hopefully April run disciplined by GTP

Next phase : ATCA Trigger Card

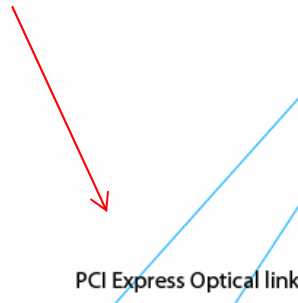
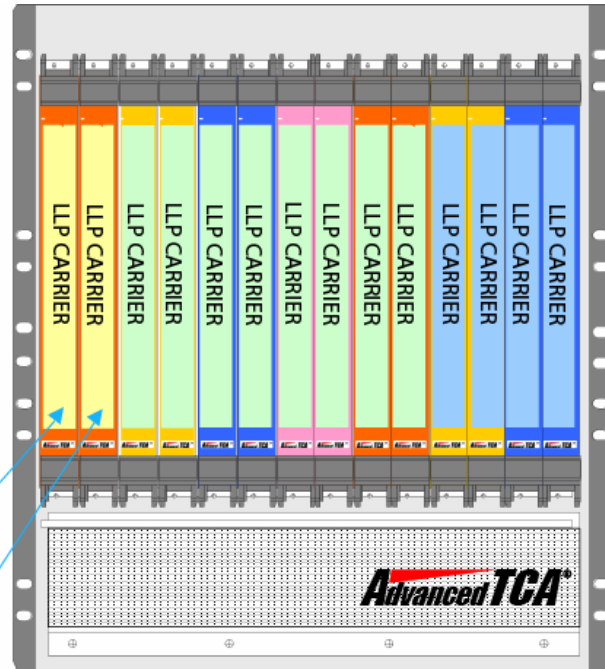
- Current scheme based on mezzanines limited to a (max) triple cluster
- Need to fanout many nodes per card
- Common design for fanin/fanout and root node
 - Shorten hardware development cycle
 - Reduce cost
- Design should start Q4 - 09

Trigger card block diagram



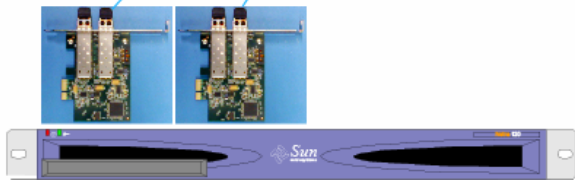
PCIe Interface card

Present situation: 2 cards x crystal



PCI Express Optical link

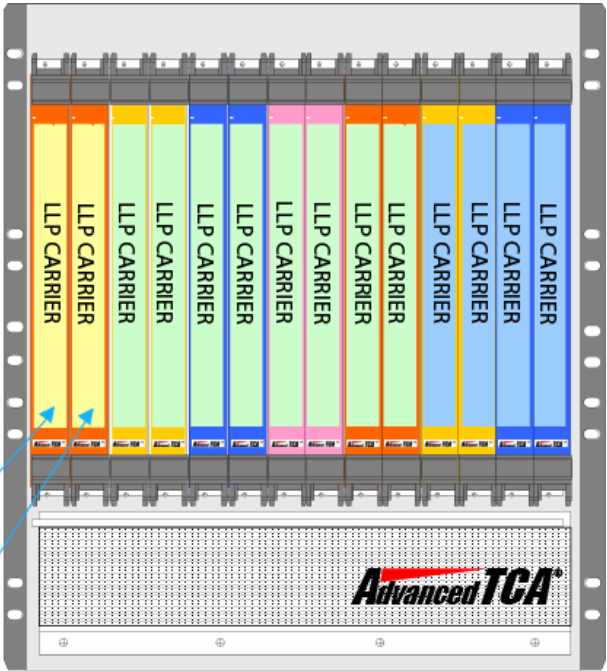
BW : 200 Mbytes/s/link – PCI Express 1.1



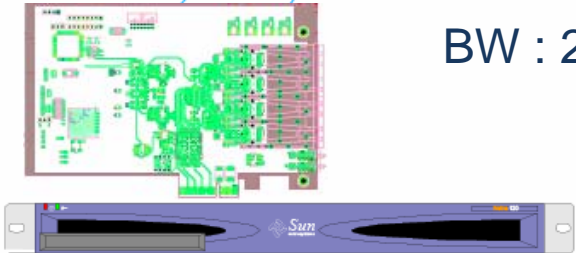
New PCIe Interface card

New configuration: 1 card x crystal

PCIe Gen 2

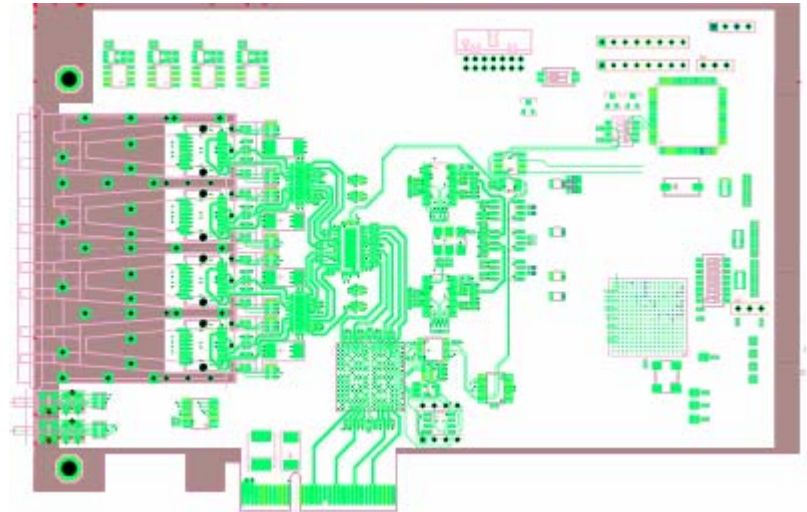


BW : 200 Mbytes/s/link



New PCIe I/F features

- Based on a Gen 2 switch
- Highly configurable
 - 4 links 1x Gen1/Gen2
 - 2 links 2x Gen1/Gen2
 - 1 link 4x Gen1/Gen2
 - 2 links 1x Gen1 + clock (Agata case)
- Mixable operation on different links
- Host interface 4x (Gen 2 – 20 Gb/s aggregate)
- Prototype currently under development



GTS Overall Status

- No improvements on the demonstrator until Q4/2009
 - J. Chavas will leave the group in two months
 - The only one left to work on firmware/slow control
 - GTS frozen to a single cluster
 - No integration of ancillaries or new Ge detectors possible
 - Lack of manpower on the firmware