AGATA PROJECT

Preprocessing Mezzanines
Group electronique CSNSM

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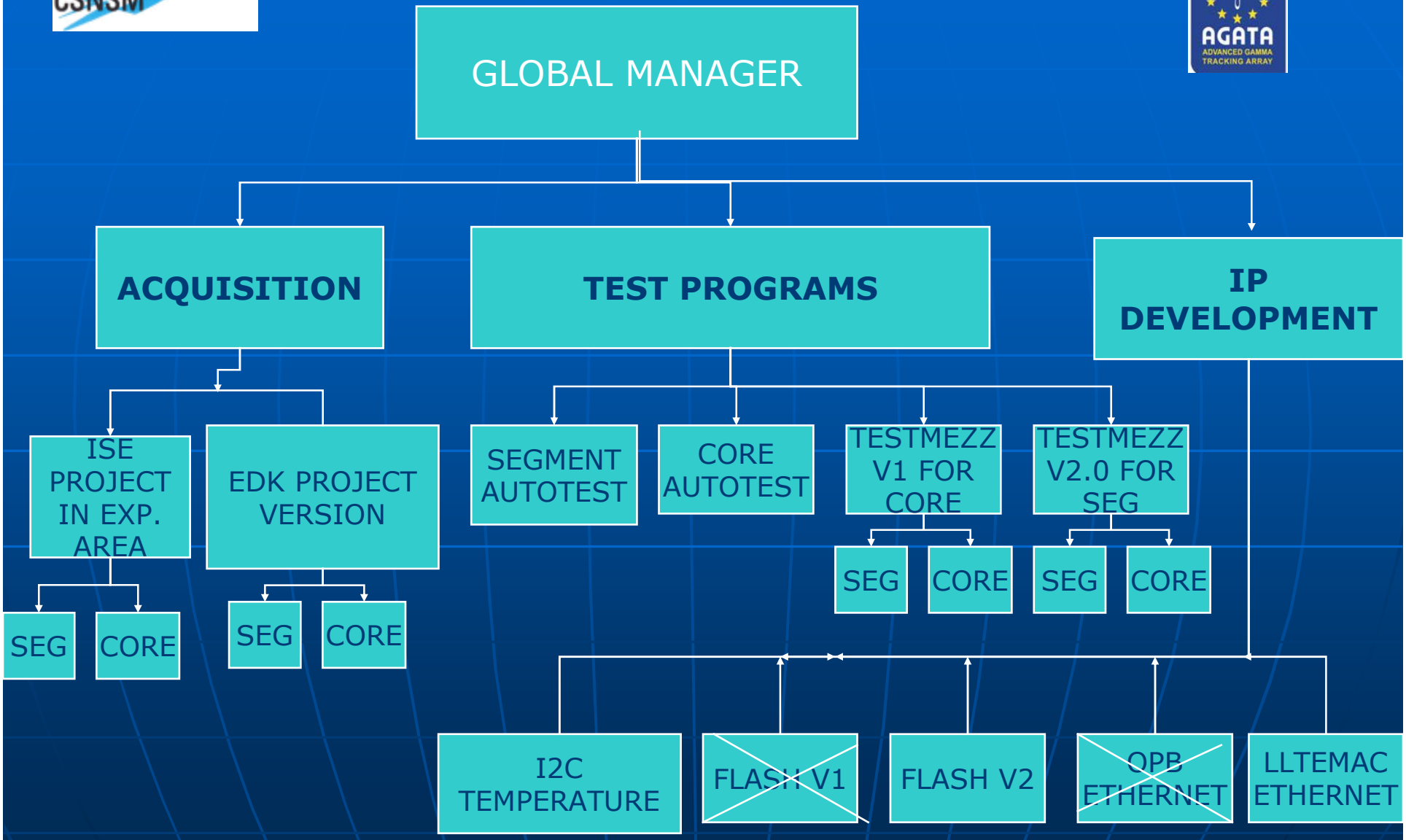
Outline

- List of work on Hardware and VHDL since last AGATA week
- Management of the VHDL
- Slow Control Integration (will be seen in SC DAQ)
- Mezzanine qualification report
- Core card Status
- CSNSM Manpower working conditions
- Pre Processing Test Bench Facility
- Production status for the Demonstrator phase
- Engineers and technicians working on Agata

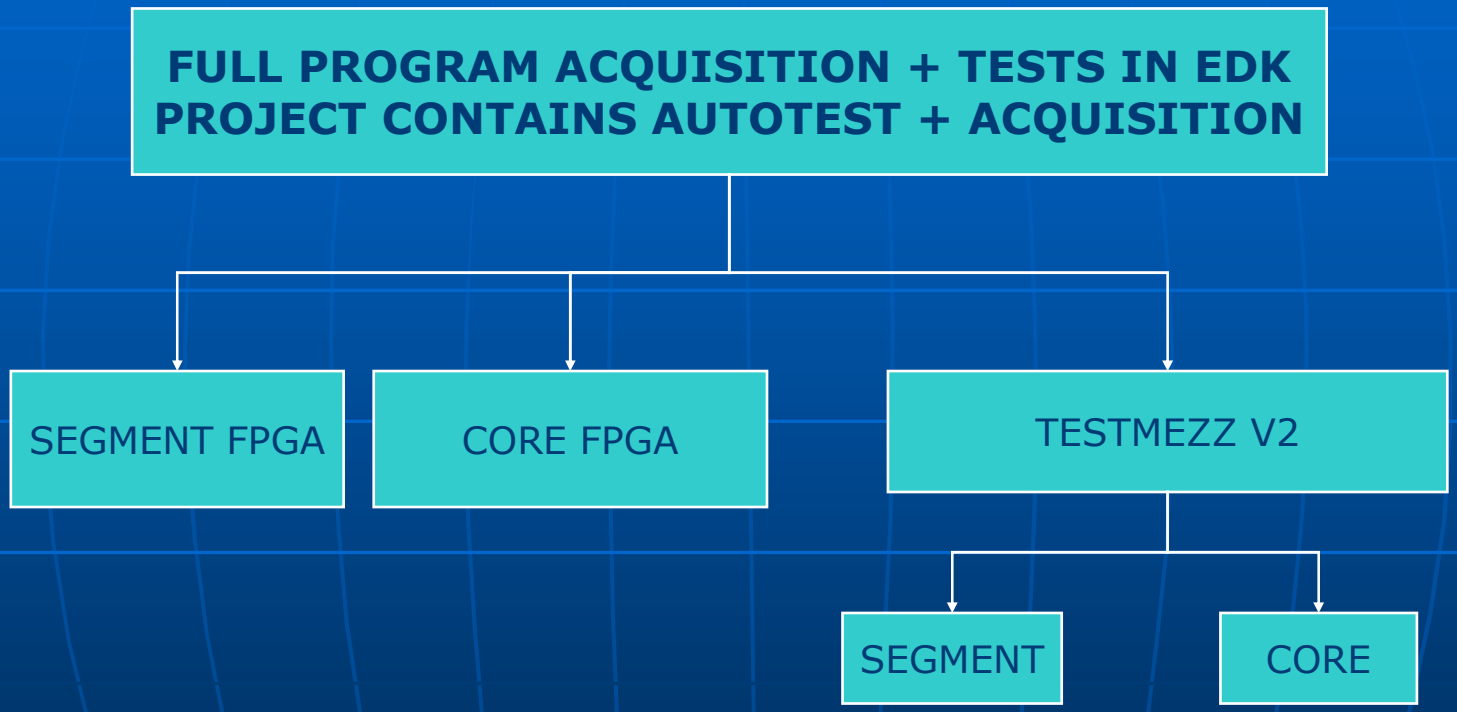
List of work on Hardware and VHDL since last AGATA week

- Qualification of clock jitter on segment and core (07/08)
- Segment card production for the triple cluster tests (09/08)
- Problem of the programmable delay lines (09/08)
- core card prototype validation (10/08)
- Starting Slow control VHDL Development (09/08)
- Enhancement of the existing VHDL acquisition (continous period)
- Adding I2C interface with the carrier card to make minimum register control for acquisition (collaboration with INFN)
- Adding new IPs to complete the mezzanine facilities (I2C Temperature measurements, slow control per channel registers, nand flash interface)

Management of the VHDL



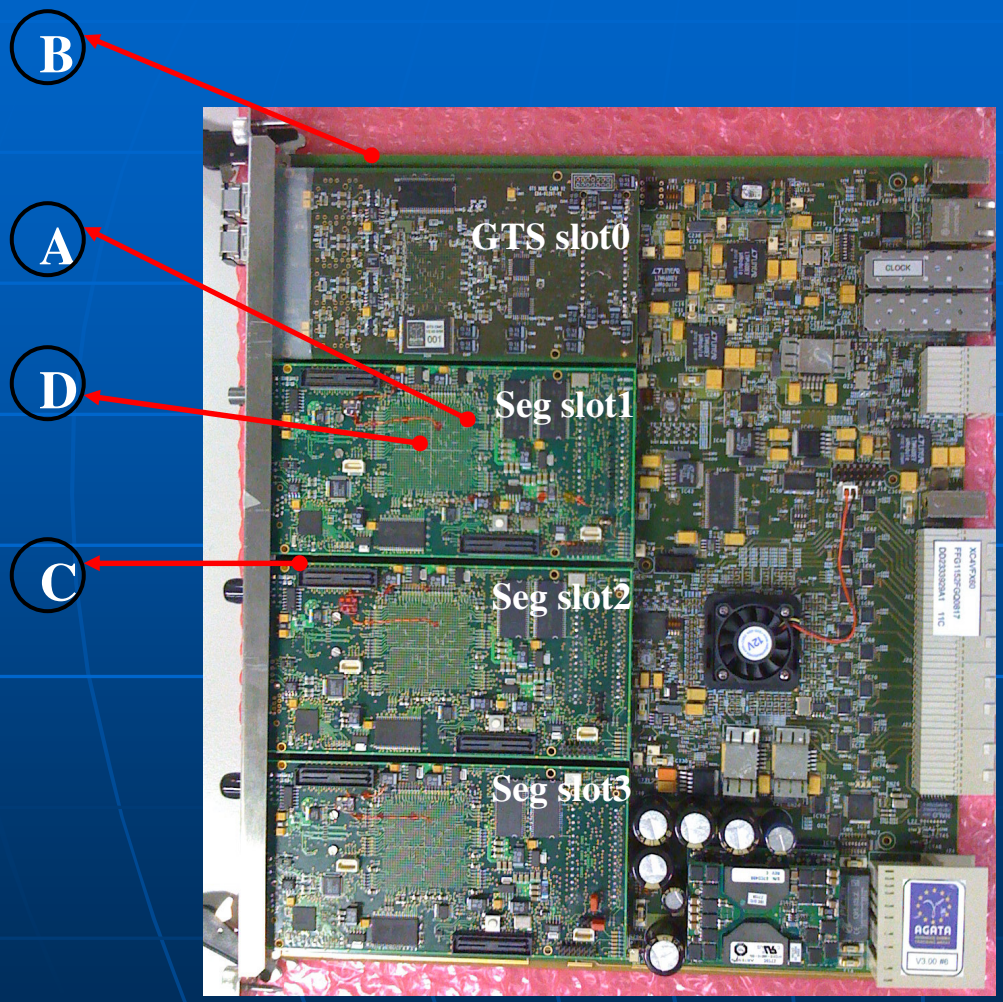
Management of the FUTURE VHDL



Mezzanine Qualification report

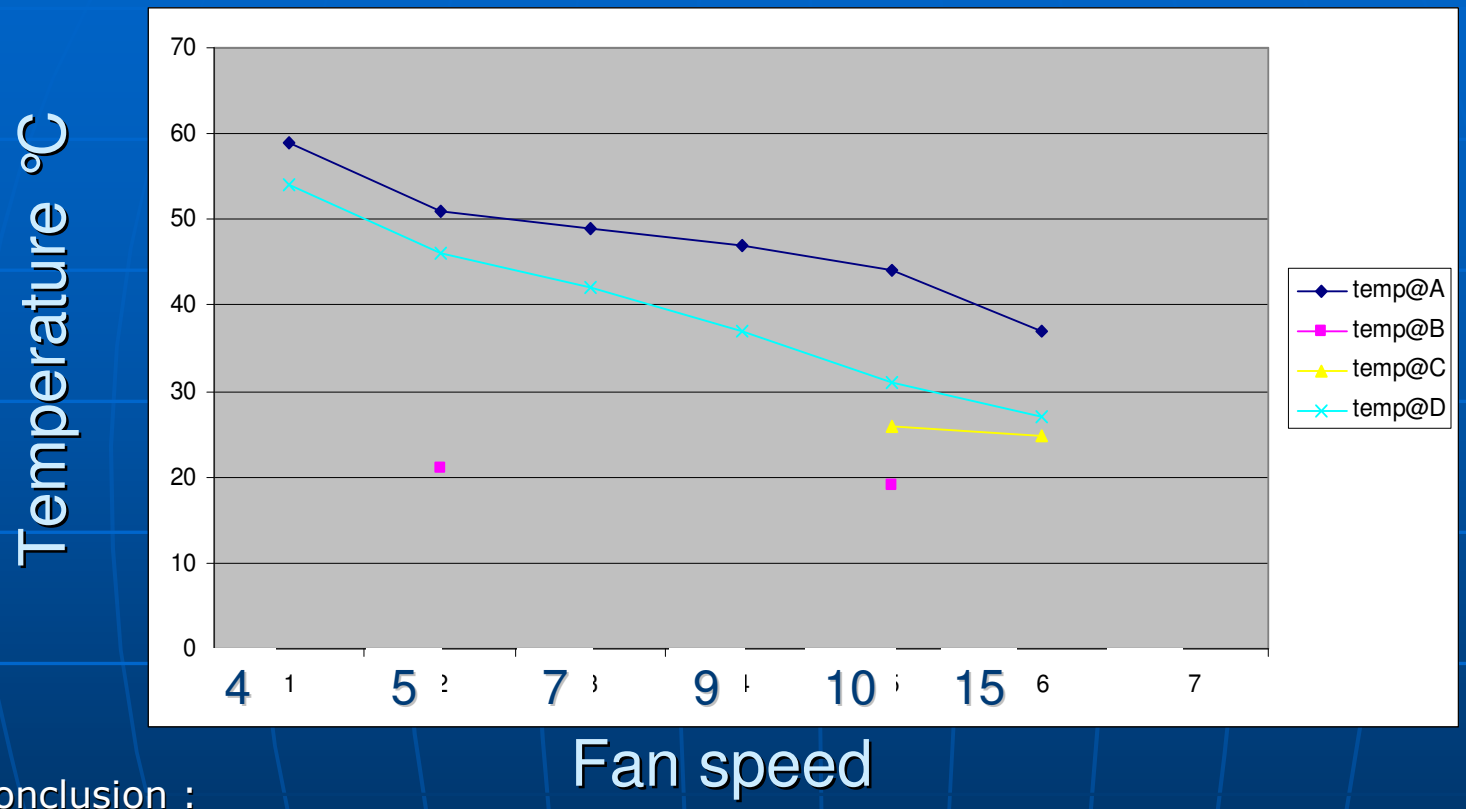
- Ramp Tests with digitizers and LFSR pseudo-random tests were made to qualify optical fiber data transfers.
- Ethernet tests on the mezzanine phy OK
- Ethernet tests on the carrier OK
  - took long time because of lack of technical support
- Temperature I2C interface tests OK
- Flash interface development
  - 32 bit address 32bit data to 8 I/O bits
  - Special VHDL interface design (no technical support)
  - Additional C programs driver to access Flash
  - New boot loader program to load Linux
  - RS232 interface to validate the SREC file transmission
  - Status is working from RS232 interface
  - Linux ENX interface is designed. Its under tests :needs some extra work 1 page loads and program stops. Tests are underway. Ready end of April to be installed in Experimental Area.

Mezzanine Burning Tests



- A : the probe is in contact with the bottom side (via an isolated piece of scotch) of the mezzanine PCB number 1.
- B : The probe measure the temperature airflow extracted from the space between the GTS-Carrier cards on the top of the Carrier board.
- C : The probe measure the temperature airflow which circulate in the space between the Segment-Carrier cards near the front panel.
- D : The probe is in contact with the bottom side (via an isolated piece of scotch) of the mezzanine PCB number 1

Mezzanine Burning Tests



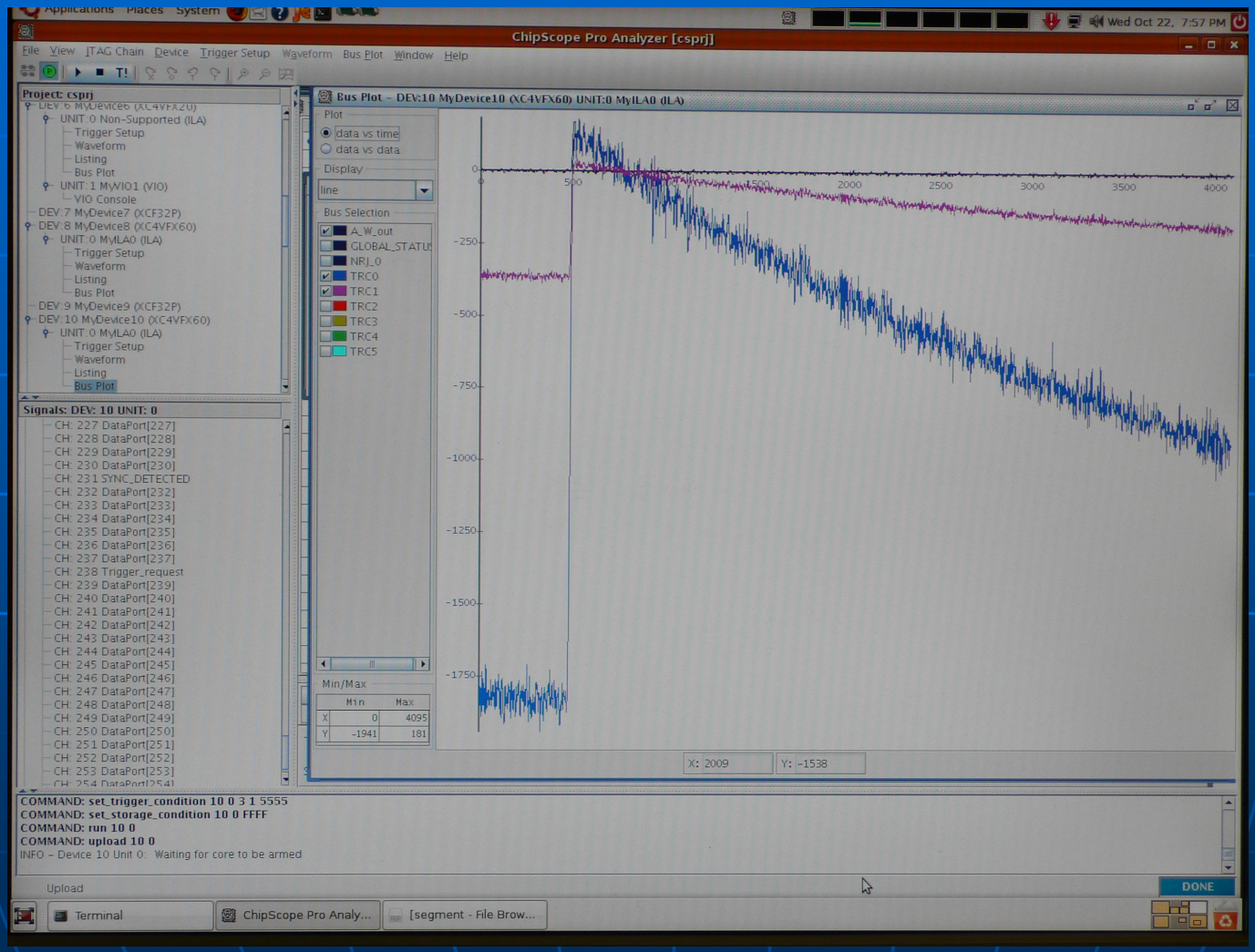
- Conclusion :

1. It is crucial to measure online all the mezzanine FPGAs temperatures and to have a feedback to the shelf manager
2. If fan is lowered or cutoff for more than 2 minutes on the preprocessing cards, there will be serious damages inside the cards.
3. This experiment was extremely useful to know the cards behavior under severe conditions.

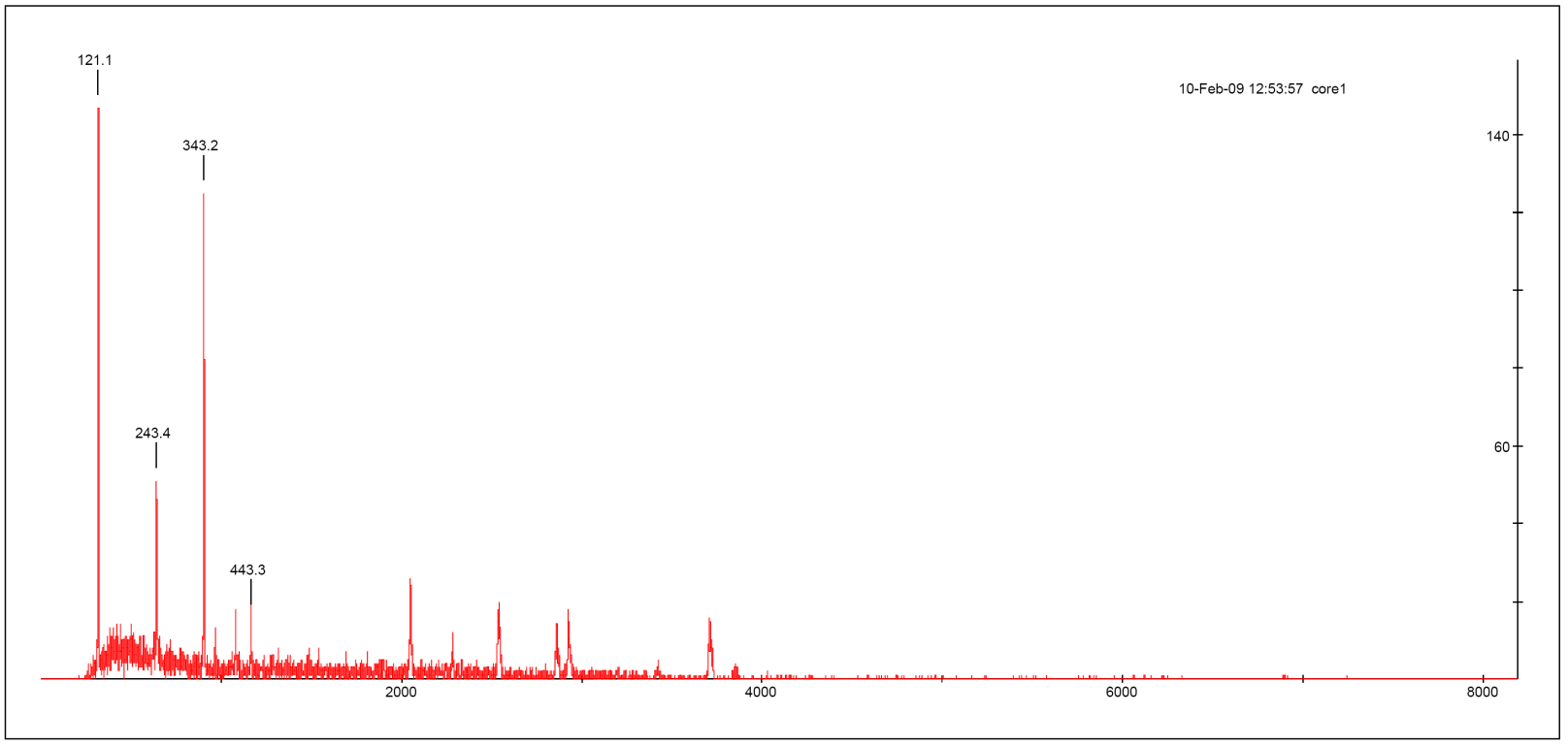
Core card Status

- 3 prototypes exists. 1 is fully tested and 2 partially tested
- Qualification is not fully done (long time acquisition to validated received data)
- All IP development by the segment card can be used for the core card since the hardawre interfaces are the same.
- Qualify core card programmable delays and clock distribution for physics necessity
- Do we enhance data quality by synchronising ADC clocks and synchro signals through core card?
- If yes core card qualification will continue
- If Not core card qualification and production for the 1 pi will stop.
- Response is needed from experimental data analysis from source and beam experiments.
- Deadline to reply to electronics team (somewhere Q3 or Q4 2009?)

Trace data from chipscope for the Core card



First preliminary spectra for the core card from source @ LNL



- This spectra does not have enough statistics.
- Core signal has oscillation not so perfect
- Data was recorded roughly but it comes from core card
- conclusion is that new acquisition is needed and comparison with segment card is essential. At least we got a humble resolution @ 121 keV of 2.3- 2.4 keV (worse @ high energie) could be enhanced

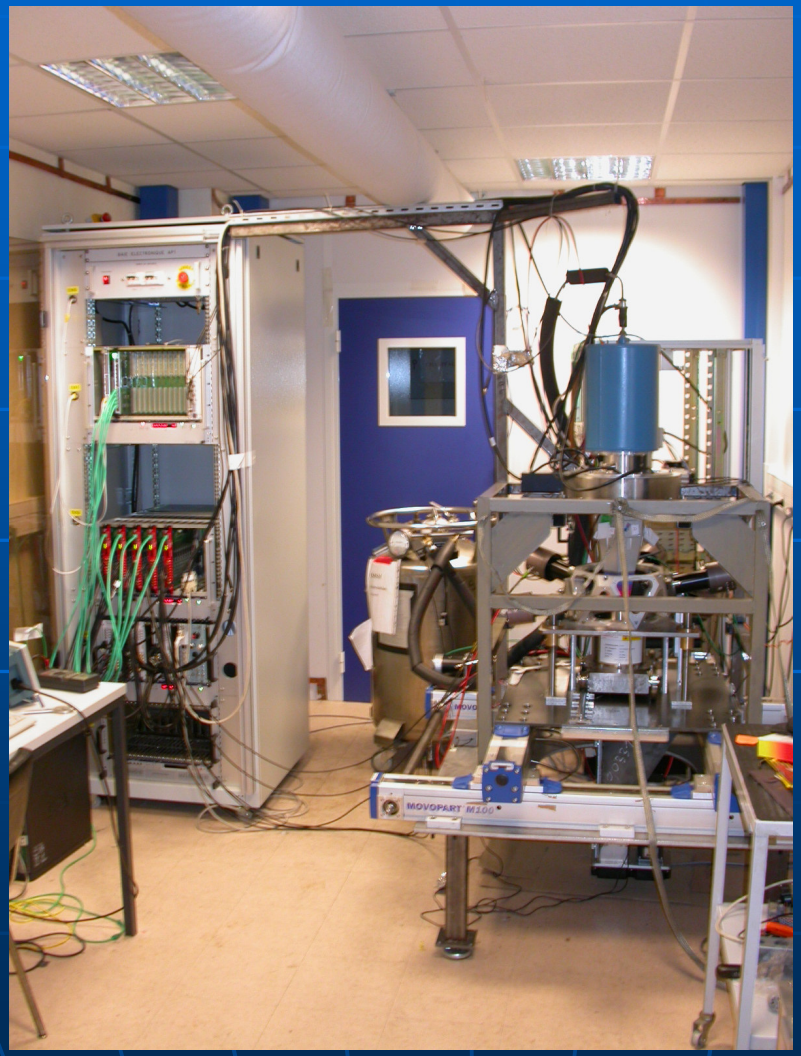
CSNSM Manpower working conditions

- All this work is done in parallel while going to Legnaro for triple cluster qualification.
- All the work is done either with test board or at the only system in legnaro. This was a real handicap to accelerate development.
- Un equivelant to 30 visits of 4 days are done @ legnaro. The financial budget was under estimated.
- It was a continuous challenge to overcome all the problems
- Lot of problems in Development tools (upgrades enhance one thing and existing code was to be modified, PC hang up often)
- No technical documentation from Xilinx. (use google to search for information on forums or other website !!!)

Pre Processing Test Bench Facility

- Orsay will produce 34 Carrier boards coupled to 140 mezzanine boards.
- ALL should be fully tested before delivery
- All installation infrastructure exists and can support fully equipped crystal detector acquisition. (CSNSM has Agata Scanning)
- No additional tests are required before installation inside AGATA hall @ LNL
- Full 100 % test coverage of AGATA preprocessing electronics
- Readout 1 complete crystal detector data
- Compare readout data with scanning data
- DAQ and SC Team are @ Orsay collaboration IPN and CSNSM

Basic Infrastructure for the PPTB (cont.)



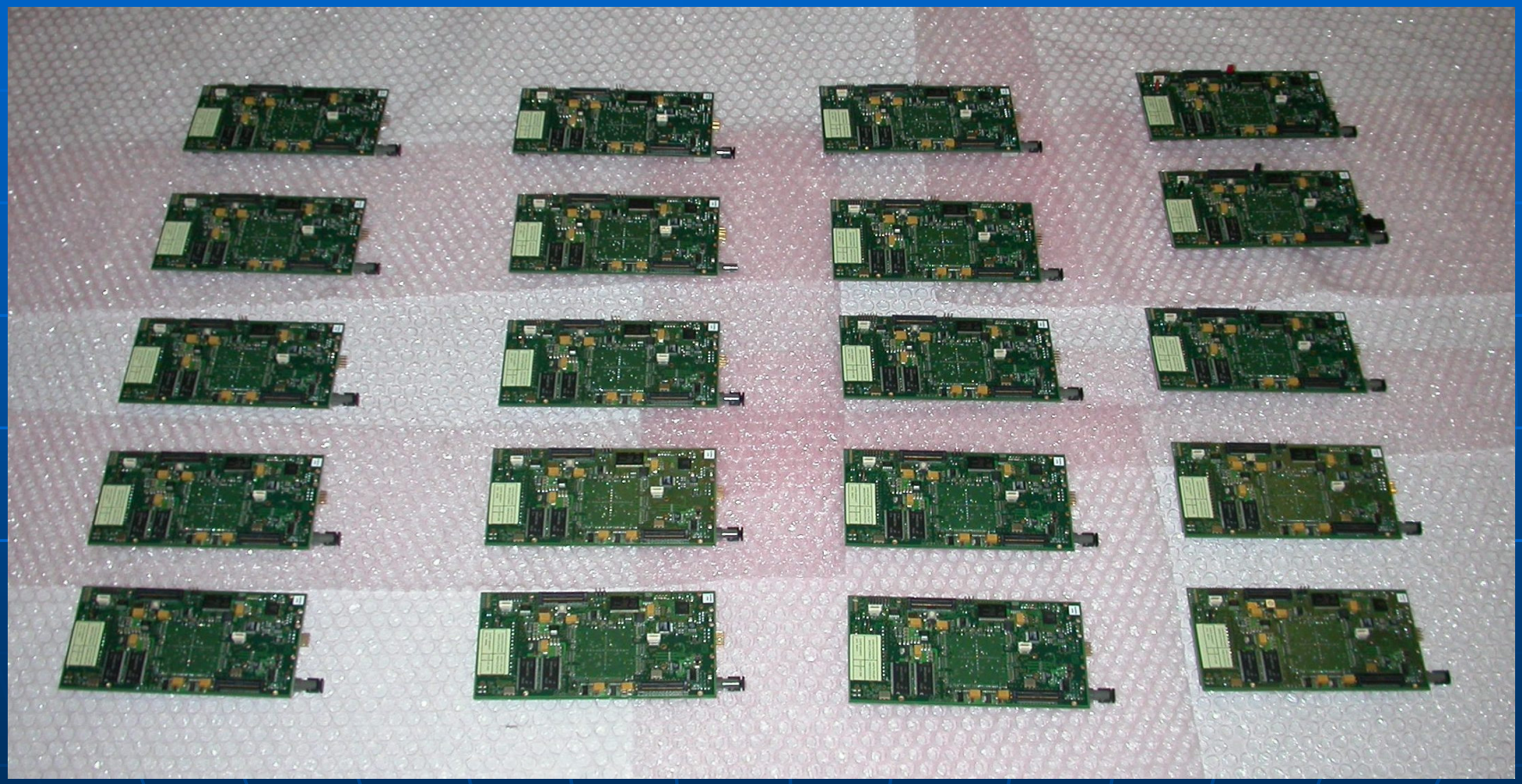
Operation &General needs of the PPTB

- Generation of 1 Agata segmented crystal data
  - Install 1 complete digitizer with the crystal
  - Install 1 ATCA crate
- Generate Trigger signals from Core triggers
  - Install 1 GTS card
- Readout 1 complete crystal detector data
  - Install 1 Narval DAQ pizza with PCI eXpress Readout
- Compare readout data with scanning data
  - Verify PPTB data with local scanning DAQ (Tigress)
- Simple Run control setup using scripts
  - Install VxWorks to control carriers and use existing configuration file.

Production Status

- Started in February instead of January. Reasons:
  - Burning tests took place end January 09,originally planned on Dec 08.
  - This delay is due to the lack of test systems
  - Priority was to finish carrier tests (finished mid January instead of November) due to assembly problems.
- Batch of 20 cards are manufactured within 7 working days instead of 14 days.
- 90 more cards will start Week15. Cards will be received by batches of 30 starting Week 19

Production Status



CSNSM AGATA Technical Staff

- HW production & Manager: D. Linget 50%
- SC and VHDL Project Manager & Spokesman : N. Karkour 50%
- SW group : N. Dosme, E. Legay 80%
- HW group : X. Lafay, B. Travers, 90 %
- Technical support : S. Leboutellier, E. Pierre 50%
- Special thanks to IPN team (X. Grave, Ch. Oziol et al.)
- Special thanks to the INFN Padova Team (M. Bellato, D. Bortolato, J.Chavaz) for their precious collaboration
- Special thanks to Daresbury STFC team (I. L.azarus, P.J. Colemansmith)