



DAQ session 9

Slow Control

Ch. THEISEN

Goal of the SC



- Define which electronic boards are present in the system
- Initialize the different boards with the correct values (write registers, execute initialization procedures ...).
- Save (onto disk) all the setup parameters of the whole electronics or a part of the electronics.
- Restore a previously saved setup.
- Monitor the hardware and more generally the whole system (data quality)
- Handle error/alarm events and pass them to the Run Control.
- Accept some simple commands (setup, go, stop, get state ...) to control all the active components.
- Global configuration of the experiment and the whole system
- Provide Graphical User Interface

Slow controlled elements



- Digitizers
- GTS Trigger Processor
- ATCA carrier boards
- GTS mezzanines
- Core & Segment mezzanines
- (Ancillary electronics)



- Different SC levels (or layers)
 - VDHL Virtex
 - PPC Virtex
 - Global config of a subsystem (carrier card, crystal, ...) with interdependences
 - Global config of the array (also with interdependences)
- ... Some part very close to the hardware, some other closer to DAQ (services, RC, GUIs, network, ...)
- Ideally, SC done by peoples very close to the hardware, therefore manpower issues.
- Coordination between FEE, RC, GUIs, ...

ToDo as discussed Feb 18, 2009



1. Vic's WSDL implementation
 2. Definition of new WSDL messages
 3. Synchronization of subsystems – sequences of actions. Document list of actions. Coordination of SC technologies
 4. Definition and implementation of the systems topology
 - 5a Save/Restore
 - 5b Global configuration of Agata from the RC.
- In parallel :
- Monitoring
 - Diagnostic : replace chipscope
 - GUIs

SC meeting yesterday



- WSDL
 - Vic's services and its extensions
- Global configuration and topology
 - scalability
 - Sequence of actions; errors management
 - Full configuration of the array and part of it
 - Solutions to manage global SC and connections to RC
 - Responsibilities
 - Dream to have a self-describing system
- Chipscope-like and traces analysis
 - Automatic traces scan at init
 - Consequences on SC
 - Sent traces from mezzanines to DAQ
 - How to display / analyse traces ... and who
- Internal diagnostic (report status)
- Quality monitor
 - Still issue

Today's agenda



- **Ch. Theisen**, Overview and goals
- **M. Gulmini**, Run Control-Slow Control integration
- **V. Pucknell**, Digitizer
- **N. Dosme and N. Karkour**, Core and Segment mezzanines SC