Miniball electronics at CERN - May 2006

Contents

[1] Nigel Warr 22 September 2006

1 Foreword

This document describes the state of the electronics used at CERN for the May 2006 setup. It is based on the one for May 2005, which in turn was based on the one for July 2004.

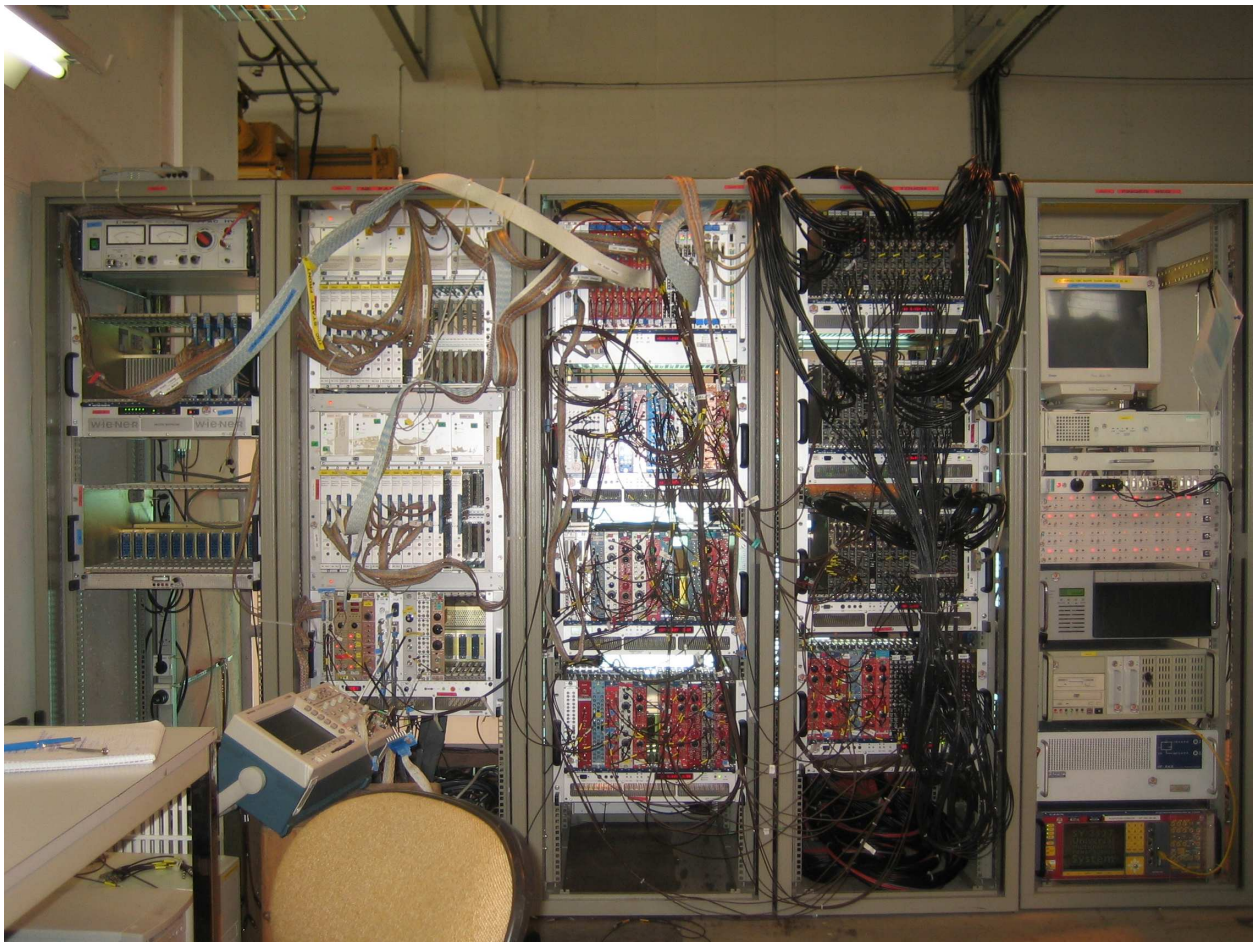

Figure 1: The Miniball electronics in 2006.

The differences to 2004 to 2005 have been indicated, notably the addition of laser on/off bits in the pattern unit and the Munich ionisation chamber, and changes in the TDC cabling. That means it is different to all previous experiments and is likely to be different to future ones. However, there should be certain similarities.

The electronics for this setup has grown gradually rather than being thought out as a single setup, so modules were not necessarily placed in the optimal position in the crates. In places, signals were duplicated due to different people building different parts of the setup and not realizing that the signal they were constructing was already available elsewhere.

In November 2004, a part of the electronics was dismounted and sent to GSI, Darmstadt, and the racks were all moved in order to allow for the building work to extend the ISOLDE hall. However, care was taken then to label things, so that they could be put back together. In May 2005, we put the things back together and it is believed that the state of November 2004 was achieved. In doing so, we noticed some changes with respect to the July 2004 setup. These all seem to be deliberate improvements.

However, the setup works, so there is no reason to change it for this campaign, but it could be improved on in the future.

Caveat: this document was produced during the setup with all the interruptions that that entails, so it probably contains mistakes. Several mistakes have already been found and corrected. There are likely to be others! Also people were still modifying the electronics while I was noting down the configuration. Use it with caution!

The main difference between the 2003 and 2004 setups is that in 2003 all of the CD was treated as one unit, whereas in 2004, each quadrant was dealt with separately. Also, in 2004 we took the ADC busy directly from the ADC module, whereas in 2003 we generated our own signal which was longer than the one generated by the module. Back then, we thought (erroneously) that the ADC was giving a busy signal which was too short and was the reason for mismatches in the number of ADC gates and the number of timestamper DGF events. In fact, the problem turned out to be due to the DGF sometimes missing the last event, so there was no reason to artificially generate the ADC busy.

Part way through 2005, a change was made to the way the TDCs were triggered. Before this change, a signal was generated from the particles and sent via an NIM to ECL converter to one of the last 16 channels of the TDC. After the modification, flat cables were taken from the MALUs giving the hit pattern in the front part of the CD, combined together in pairs (i.e. 8 signals from 16 rings). However, they weren't cabled very logically, so that for the ADCs had the front part of the CD on channels 0 to 15 and the back on 16 to 27 with 27 to 31 unused, but the TDCs had the back of the CD on channels 0 to 11, 12 to 15 unused and the front on 16 to 23. For 2006, we have adopted the same convention for the TDCs as for the ADCs, so the front is first and the back comes after. Consequently, we removed the NIM to ECL converter that was used for this.

In 2005, we also used the Miniball HV main frame to produce the high voltage for the beam dump detector. Prior to that we used a NIM power supply.

Another minor change in 2006: we moved the TDCs one slot to the left and put the ADC for the ionisation chamber to their right, rather than having the ionisation chamber ADC between the ADCs and TDCs for the CD. We also swapped a VME scaler with NIM inputs and the adjacent VME scaler for the PPAC.

2 Notation

I have used the notation "R2.C4.S13" to mean rack two (starting at 1 nearest the wall) crate four (starting with 1 at the top), slot 13. Similarly "R2.C4" means all of crate four of rack two. In the diagrams, the location of the modules is indicated in magenta.

3 The CD cabling

There are two crates of RAL109 shaping amplifier modules. The top one (R2.C1) is for the 16 front rings and the bottom one (R2.C2) is for the 24 back sectors.

The analogue outputs of the RAL109s for the front go directly to channels 0 to 15 of the CAEN V785-AG VME ADCs in R3.C1.4-7 (i.e. the lower part of the ADCs).

The analogue outputs of the RAL109s for the back also go directly to channels 16-31 of the same ADCs, but since we only use 12 signals (we combine the 24 sectors per quadrant of the back of the CD into 12 signals, by connecting them pairwise - this is done in the hardware) there are some channels spare. By picking off a couple of the wires from these cables, the CD PAD detector (another RAL109 in R2.C1) and the laser power (from the laser control box) are also put into the ADCs.

The ECL outputs of the RAL109s for the front are connected into the four MALU modules (R1.C2.S17,19,21, 23). From there, the ORO signals are connected via a flat cable, where the ends have been split at the MALU end, to an ECL to NIM converter (R2.C3.S1). Also, flat cables connect the outputs of the MALUs to the CAEN V775 32-channel TDCs in R3.C1.8-11 (channels 0 to 15, i.e. the lower part).

For the back sectors, the ECL outputs are connected directly to the same TDCs on channels 16-31 (i.e. the upper part).

Additionally channels 0 and 1 of the laser box are connected to channels 28 and 29 of the quadrant 1 ADC (R3.C1.S4). It looks like the latter one is the laser power.

The signals from the PAD detector come from a different RAL109 in R2.C1 and should each be connected to channel 30 of the ADCs (R3.C1.S4-7). This is done by splitting off two channels from the flat cable and connecting them individually. However, because of the modification to the cable for quadrant 1 in order to add in the laser power (actually, a new cable was made - it is blue and white, while the others are multicoloured), it looks as though quadrant 1 of the PAD detector isn't connected any more.

Probably, we should make a new cable for quadrant 1, with both the PAD and the laser power.

4 The delayed CD quadrant signal

From the CD we need to generate logic signals to indicate when an event has occurred in a given quadrant. Note that in previous setups we treated the whole CD as one, but now we treat it as four independent quadrants.

For each quadrant, we take the logic output from the RAL 109 shaper amplifiers via a flat cable to four CAMAC MALU units. Note that although these are CAMAC modules, we do not need to program them, so they are in a crate without a CAMAC crate controller. They just take their power from the CAMAC crate.

Each MALU gives a differential ECL *ORO* output (this is just an OR of all the inputs) and these signals for all four MALUs are combined on a single flat cable and sent to an ECL → NIM converter. From there, the signal for each quadrant goes into one quarter of a 4x4 fan-in/fan-out module and then is used to start a dual timer.

We use two copies of the signal from this fan-out.

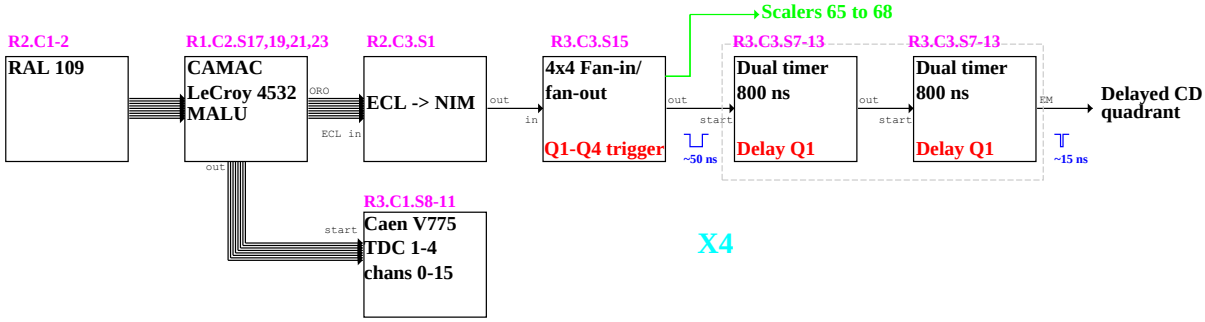

Figure 2: The generation of the delayed CD quadrant signal. This is done for each of the four quadrants of the CD.

- One goes to a scaler. We use scaler 65 for quadrant 1, scaler 66 for quadrant 2 etc.
- One copy is delayed by 800 ns to generate the delayed CD quadrant signal.

We want to delay this signal by 800 ns, but the CAEN dual timers have the property that if a second signal arrives during that time, the end marker comes 800 ns after the **second** signal, not the first. So we use half of a dual timer to generate a signal which is 800 ns wide and then use that to start the second half of the same module also set to 800 ns (so both start more or less simultaneously, but the delaying of the end marker is suppressed). We then take the end marker from the second half of the module. There are probably better ways to do this. In all probability this behaviour of the dual gate is a feature but it doesn't seem to be possible to turn it off and the manual is utterly useless. Perhaps a different kind of gate generator would be better, or a discriminator followed by a gate generator. In future years we should really rethink this part.

For all four quadrants, we use four MALUs, one ECL → NIM converter, one fan-in/fan-out module and four dual timers.

Note that the RAL109s and the NIM crate containing the NIM → ECL converter are in the CD electronics rack, and the CAMAC crate with the MALUs are in the leftmost rack.

Previously, we took a third copy of the signal from the fan-out, passed it through a NIM to ECL converter and used it to start a TDC channel for each quadrant. Some time in 2005 this was changed and now, we take an additional flat cable from each MALU to the corresponding TDC so we have a hit pattern rather than just the OR.

5 Generation of the gamma gate

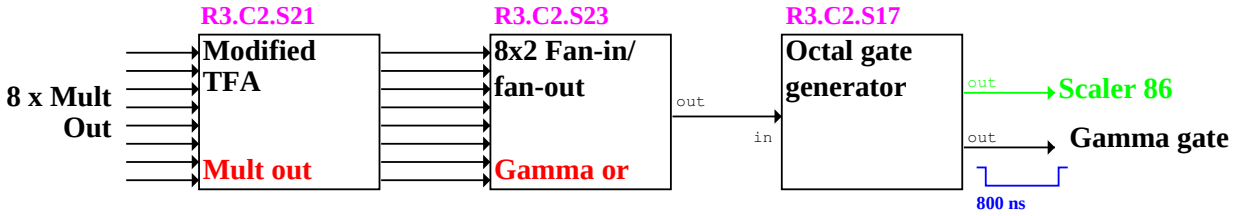

Figure 3: The generation of the gamma gate. This is the logical OR of all the signals from the Ge cores.

We need to generate a signal indicating that one of the Ge detectors has an event. To do this we take the Mult Out (35 mVolt per hit) from the DGF having the first core signal and put it into the Mult In of the next DGF with a core signal (i.e. the third DGF) and from its Mult Out to the DGF with the third core. We then send this signal (i.e. one for each of the eight clusters) to a specially modified TFA (which contains eight Ge preamplifiers set to saturate with a 35 millivolt signal and generate a -0.8 Volt NIM output). In other words, the special module simply converts the 35 mV per hit signal into NIM logic. This signal is passed into a fan-in/fan-out.

This signal is used to generate the particle-gamma coincidence. Note that its width is determined by the DGF paramter *FTPWIDTH*.

6 Generation of triggers

The delayed CD quadrant signal for each quadrant is passed to a fan-in/fan-out unit (a different quarter of the unit for each quadrant) and for each quadrant, we use three copies of this signal.

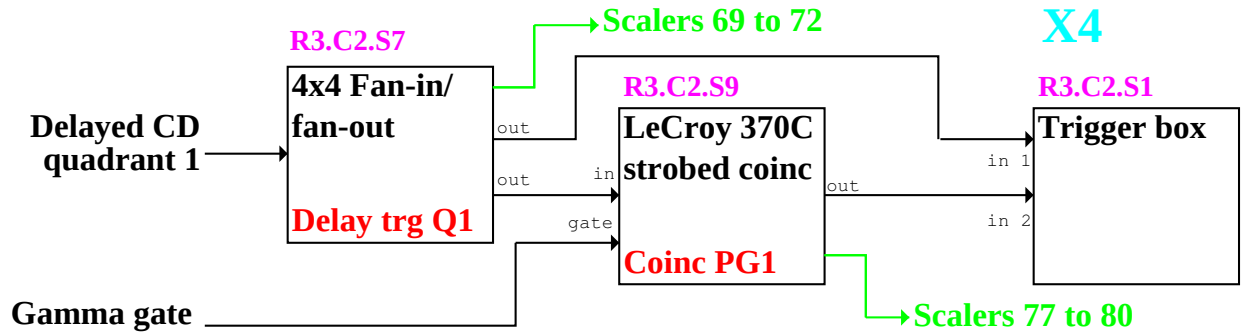

Figure 4: The generation of the triggers. The gamma gate is common to all four quadrants of the CD, but the rest is repeated for each quadrant with the second quadrant using channels 3 and 4 of the trigger box, the third using 5 and 6 and the last quadrant using the two remaining channels 7 and 8.

- One goes directly to the trigger box where it is downscaled (downscaled particles).
- The second goes into a strobed coinc unit and from there to the trigger box. The strobed coinc unit gates each input (one for each quadrant of the CD) with the gamma gate (see section 5). This gives the particle-γ coincidence.
- The third copy goes to a scaler.

Scaler 69 has the delayed trigger for quadrant 1 and scaler 77 has the particle-γ coincidence for that quadrant. Scalers 70 and 78 have the corresponding signals for the second quadrant etc.

7 Generation of the DAQ dead signals

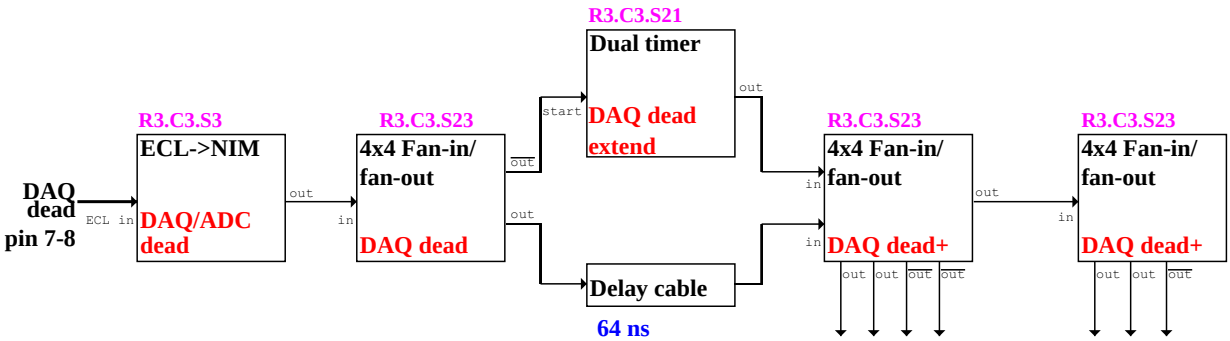

Figure 5: The generation DAQ dead signals.

The VME trigger module has an ECL output indicating that the DAQ is dead on pins 7-8 (note that pins 1-2 are the lower ones and 15-16 the upper ones). This goes through an ECL to NIM converter, after which it is split into two. One part is delayed by 64 ns and the other part is used to start a gate at the end of the DAQ dead time. The idea is to extend the DAQ dead produced by the VME trigger by a fixed amount. If we were to do this without the delay, we might get a short glitch where it goes not dead between the end of the output from the VME trigger module and the beginning of the extension. After that it is fanned out.

This bit was changed quite a lot between July and November 2004. We use seven DAQ dead signals, three of which are inverted. These come from the top two halves of the fan-in/fan-out in R3.C3.S23. The four normal outputs are used to veto the LeCroy 465 AND modules in R3.C2.S13 and R3.C2.S15 (one for each quadrant of the CD - note that the ANDs are triple modules, so the three quadrants are on one module and the fourth on the other). The three inverted outputs are used to generate the "not busy" signal (R4.C4.S11), the "DAQ trig if DAQ not busy" (R3.C2.S15) and the "Ion and not DAQ dead" (R3.C3.S19).

8 Generation of the DAQ trigger

We use the DGF SYNCH to trigger readout (having ensured that we force a SYNCH at the end of the on/off window etc. - see section 20) However, if we send a DAQ trigger while the DAQ is busy, the trigger module

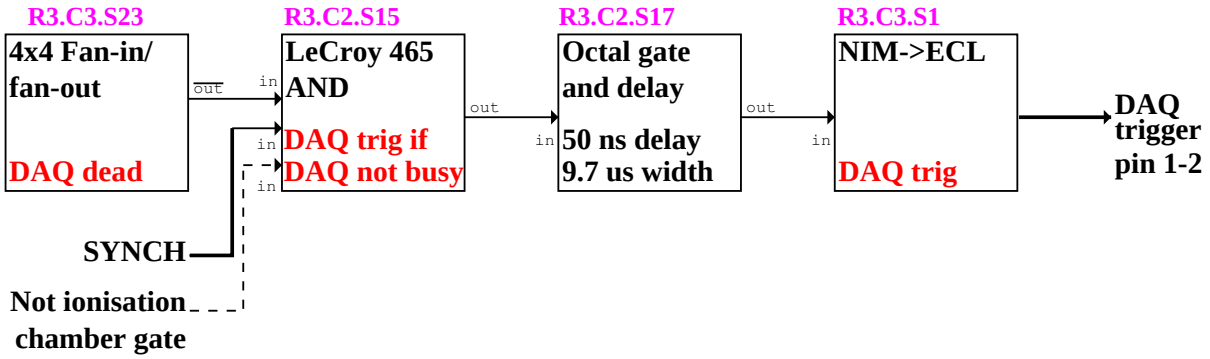

Figure 6: The generation DAQ trigger. The ionisation chamber part is shown dashed because it was not present for all experiments.

ignores it, so we need to postpone the DAQ trigger until the DAQ is no longer busy, otherwise it hangs. Since the SYNCH remains set until readout occurs, we AND this signal with the inverted DAQ dead signal, so that the moment we have both SYNCH and the DAQ is live, we generate a DAQ trigger.

The NIM → ECL converter module is the same one used for the ADC busy lines and we have a special flat cable which connects the four ADC busy lines and the DAQ dead output from the VME trigger module to different channels of this unit. We use the first trigger (pins 1-2, which are the lower ones of the ECL input on the VME trigger module).

It seems that between July and November 2004, this bit was changed a little, presumably to prevent deadlocks in the DAQ.

9 Generation of the ADC gates and the TDC stops

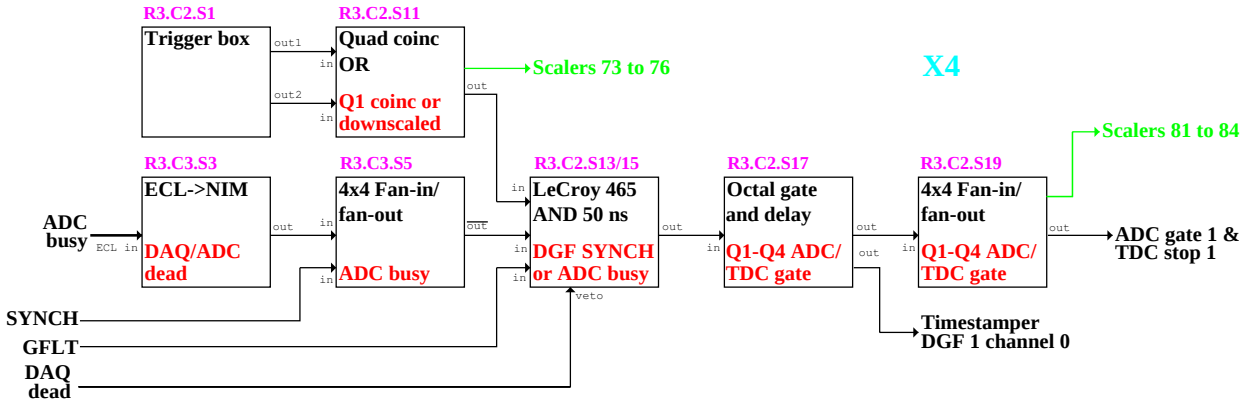

Figure 7: The generation of the ADC gates and TDC stops. Note that we have separate gates for each quadrant of the CD. This diagram shows the connections for the first quadrant. For the second quadrant we use channels 3 and 4 of the trigger box and so on.

In 2003 the ADC gate and TDC stop was the same for all parts of the CD, but in 2004 we changed it to have separate gates for each quadrant.

We want to generate an ADC gate, a TDC stop and a signal for the timestamper DGF corresponding to a given quadrant (four separate gates, four separate stops and four timestamping DGFs) all of the following conditions are satisfied:

- The trigger box gave a signal for that quadrant. Note that we can have both downscaled particle and particle-γ coincidence for the quadrant and these need to be ORed together.
- We are in the on window or the off window. This is the equivalent of the GFLT signal sent to the DGF.
- The ADC for that quadrant is **not** busy.
- The DGF is **not** busy (indicated by the DGF SYNCH signal).
- The DAQ is **not** dead (indicated by the VME trigger module).

The ADC busy signal is provided via a special flat cable which takes the ECL signal from each ADC to a single ECL → NIM converter. Note that the DAQ dead signal coming from the VME trigger module is also on the same cable and uses the same ECL → NIM converter.

Note also that in 2003 we generated an artificial ADC busy which started at the same time as the real one, but lasted longer. In 2004 we used the real ADC busy signal.

The ADC gate is taken directly from the fan-in/fan-out module at the end of figure 7 and sent to the CAEN V785 ADC gate input. Then another cable goes from the gate output to the TDC corresponding to the same quadrant.

Note that the width of the output of "DGF SYNCH or ADC busy" (R3.C2.S13/15) needs to be set to about 50 ns, not for the sake of the ADC gate and TDC stop, whose signal width is determined by the gate generator, but because these signals are ORed together to make the "Si OR" signal which is used as the pattern unit's control signal. Since there is only a fan-in/fan-out between the "DGF SYNCH or ADC busy" and the pattern control, it is here where we set the width for the signal going into the pattern unit, which needs to be at least 50 ns.

10 Generation of the EBIS window

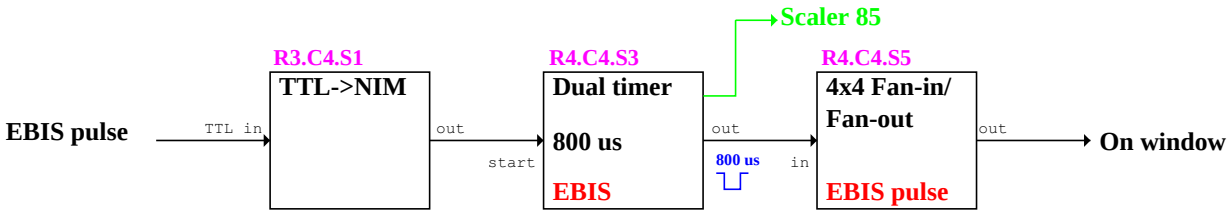

Figure 8: The generation of the EBIS window (on window)

Note: The "EBIS window" is the window provided by a signal from the EBIS saying there is a bunch of particles incident on the target. The terms "on window" and "off window" refer to two measuring periods of the same length, one on beam the other off beam. Consequently "EBIS window" and "on window" are synonymous terms.

A TTL signal is sent from the EBIS which after conversion to NIM is used to generate an 800 μs gate. The length of this gate needs to be set for the particular experiment to match the opening time of the EBIS gate.

For some reason, in 2006, we found that the dual timer was sometimes triggering on the trailing flank of the EBIS pulse as well as the leading flank, so we put it through a discriminator with a width longer than the width of the signal sent to us from the platform. Note that in this particular case, the pulse coming from the platform was 1.2 ms long, while the EBIS gate was 800 μs long. There was no point in increasing the EBIS gate to 1.2 ms, because there were no particles during that time.

11 Generation of the off window

We want to open one window when the EBIS gate is open (the on window) then read out the data and then open a second window (the off window) in the gap between EBIS pulses and read that data out in time to be ready for the next EBIS pulse. The on window and off window must be of equal length, so the off window length needs to be set to same as the EBIS gate.

When the EBIS signal comes, we send a 3 μs pulse to the timestamping DGF (note that this was 5 μs in 2003) and start a gate which is closed by the end of readout (the readout being forced at the end of the on window). We also start another gate, called "max on/off window", which is closed before the next EBIS pulse (12 ms in this case, but again this has been 10 ms or 12.25 ms in other experiments). This is used to truncate the off window, so we should also allow some time for reading out the off window data, in order to be ready to acquire when the next EBIS pulse comes. However, normally, it should be possible for the off window to close and readout to complete long before the next EBIS pulse.

Note that the length of the max on/off window should be checked for each experiment. It has to be long enough that there is an on window for each off window, but short enough, to make sure that the off window never gets in the way of the next EBIS pulse (only an issue at high repetition rates).

You can check this easily on the scope by triggering with "EBIS pulse" and looking at "max on/off window" and "GFLT". You should then see one GFLT pulse when the EBIS pulse comes and a second one after it, but before the end of the max on/off window. If max on/off window is too short, this second pulse is

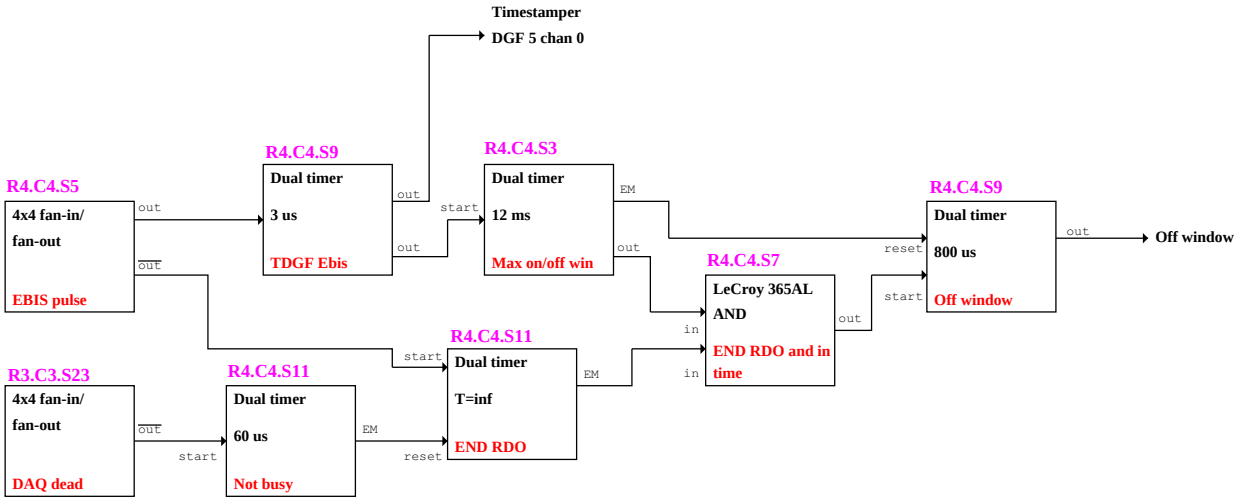

Figure 9: The generation of the off window

suppressed (N.B. the DAQ must be running too, since it is the readout after the off window, which triggers the on window).

In the setup, we use the fact that the end of the on window triggers readout, causing the DAQ to become dead for a while, so we wait until the DAQ is not dead again after the on window.

We start the off window 60 μs after the end of readout (obtained from the disappearance of the DAQ dead signal) to allow the ADCs and TDCs time to start. Note that originally, 1 μs but it seems that this is not enough time for everything to be ready. Since we have 12 ms in which to open the window, this extra delay isn't a problem. Until we increased this value, the DAQ would hang from time to time. Afterwards it didn't hang nearly as much.

The on window and off window should be of equal length. It is possible to have an on window without an off window, but not the other way round, since the off window is triggered by the first readout within about 12 ms after the on window. Consequently, if there is no on window, the off window also disappears. You should try to avoid this, if possible, by setting the max on/off window appropriately.

To set the two windows to the same width, the easiest thing is to look at the GFLT signal on the scope and if they are not the same length, you will see one width half the time and another the rest of the time, so the trailing edge of the pulse has two vertical lines. When it is correct, you only see a clean NIM pulse.

12 Generation of the on/off window

The on/off window is simply the logical OR of the on window and the off window. It is used to generate the GFLT, so the terms "on/off window" and "GFLT" are synonymous.

13 The generation of the GFLT

The global first level trigger (GFLT) signal which is sent to each DGF is the same thing as the on/off window. We use two 3 fan-in 39 fan-out modules to distribute the signal.

Typical times would be 800 μs on window then about 3.2 ms readout and finally 800 μs off window. The on and off window lengths should be equal and fixed. The readout time varies depending on the events.

14 The DGF BUSY/SYNCH loop

The DGF BUSY/SYNCH loop is made using two 39-fan-in/3-fan-out modules and two 3-fan-in/39-fan-out modules. We take all the BUSY outputs from the DGFs and feed them into the fan-in inputs and then take the outputs to the fan-outs and send the result to each SYNCH input. In this way, if any one DGF is BUSY, the SYNCH line is set to logic one and if all the DGFs are acquiring it is logic zero.

15 Note about special signals

We get several signals from different parts of the REX ISOLDE setup. When ISOLDE is running, we get a T1 signal when a bunch of protons hits the ISOLDE target, then a T2 signal when the gate is opened allowing beam from ISOLDE into REXTRAP. Since these two signals are correlated one-to-one with a fixed

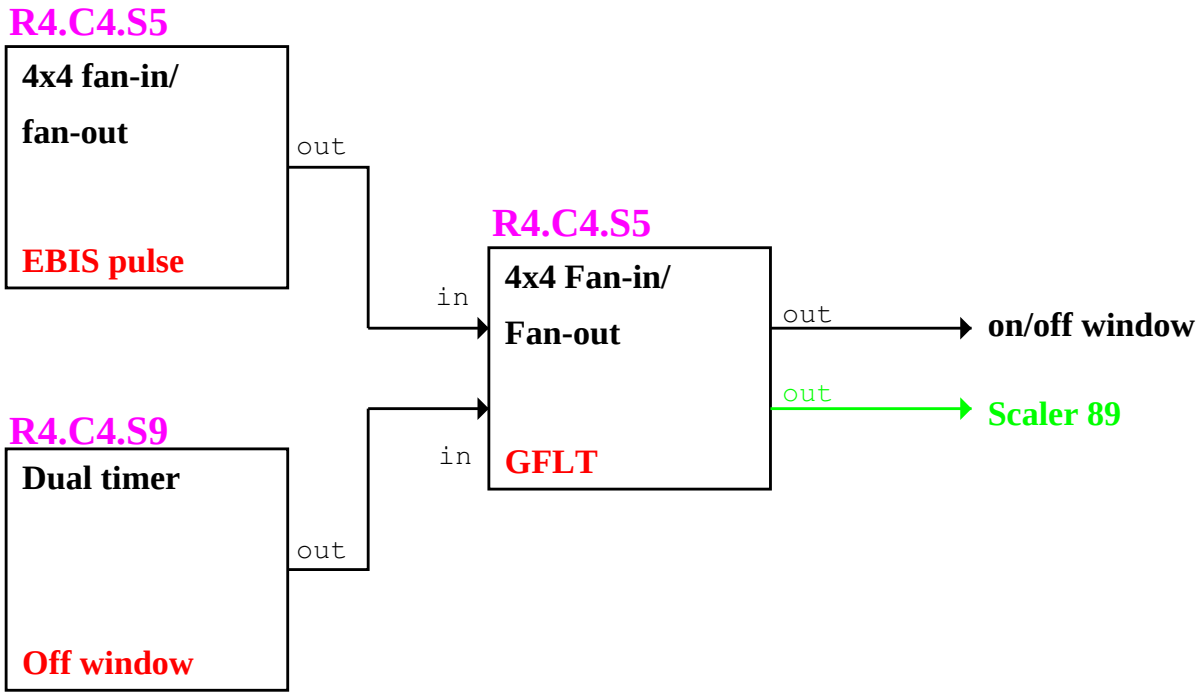

Figure 10: The generation of the on/off window

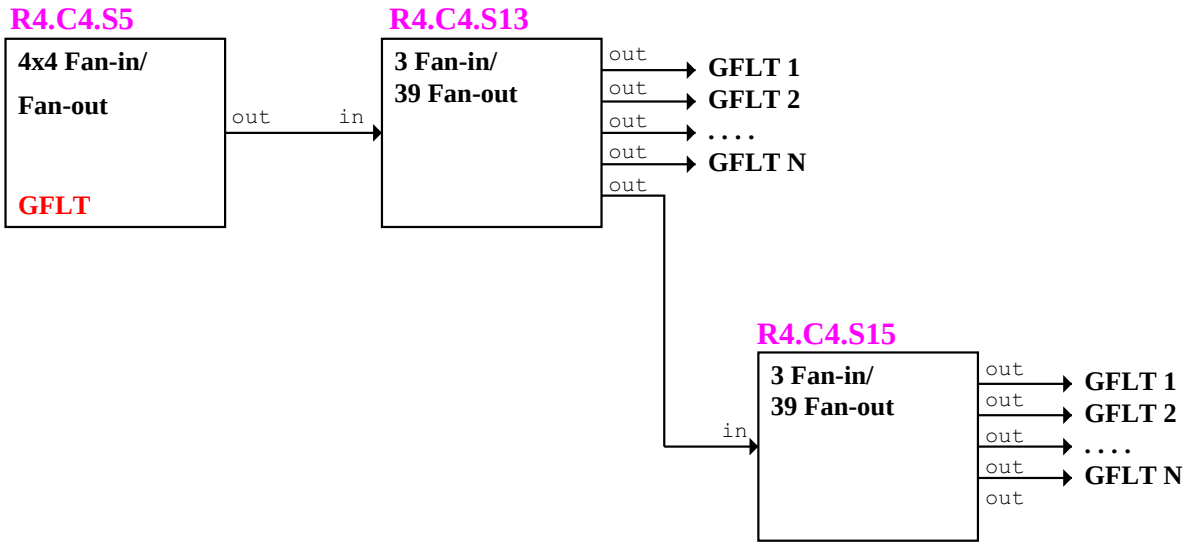

Figure 11: The generation of the GFLT from the on/off window

time delay between them, it is not necessary to have both. If the laser is running in on/off mode, we get a signal indicating laser on or laser off (sent into the pattern unit).

Note: The T1 and T2 signals are different for each separator (HRS and GPS). You need to hook them up in the ISOLDE control room for the appropriate separator.

The individual bunches of protons hitting the ISOLDE target form part of a supercycle and we receive the PS signal indicating the start of each supercycle. Comparing the T1 pulses to the PS signal indicates how many bunches we receive in each supercycle.

Once the ions have been trapped in the REXTRAP and ionised in the EBIS, the EBIS gate is opened to allow them into the REX accelerator. We receive the EBIS gate signal which indicates when ions are released from the EBIS and which is directly correlated to our beam. Consequently, we use this signal to generate the on-beam window.

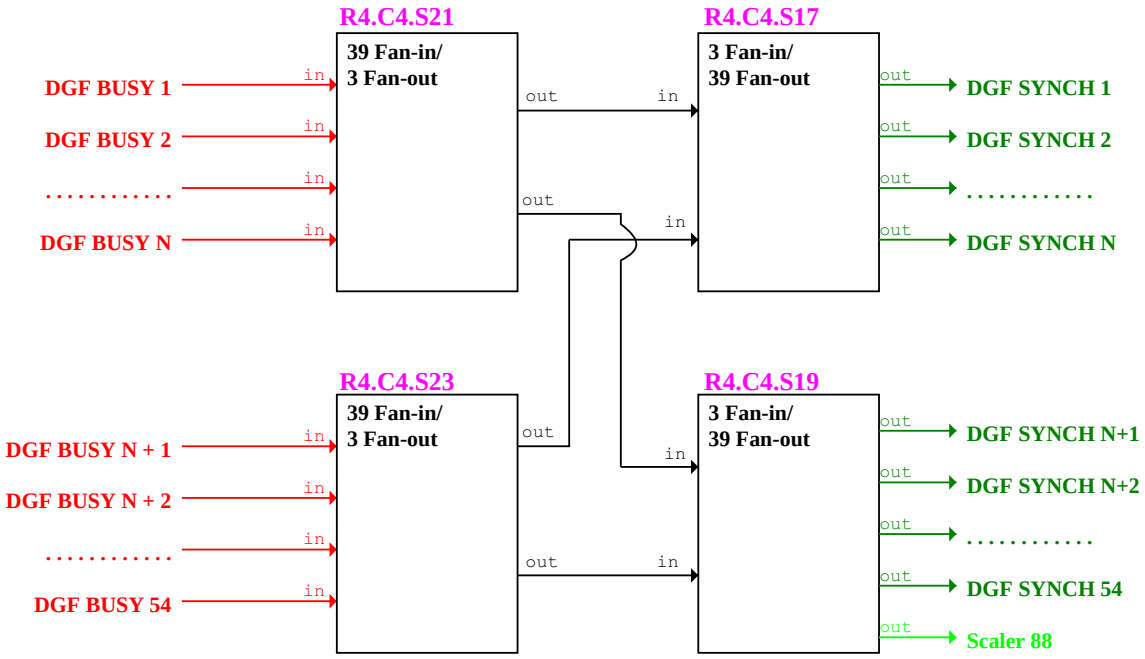

Figure 12: The DGF BUSY/SYNCH loop

16 Generation of the T1 timestamp

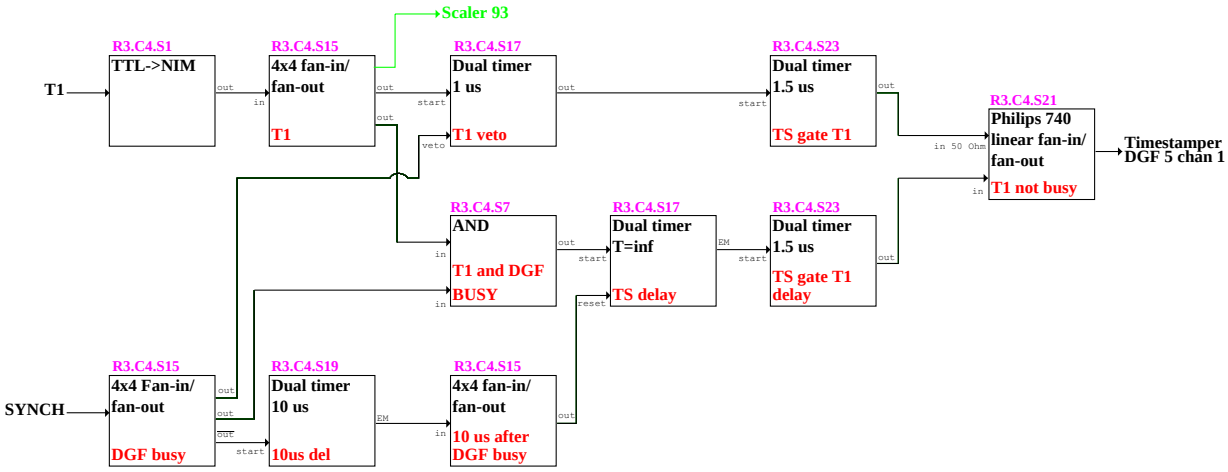

Figure 13: The generation of the T1 timestamp

We want two signals:

- the timestamp of the T1 signal itself , which we obtain by converting it from TTL to NIM and then generating a gate which we send via a linear fan-in/fan-out to the DGF but vetoed by the DGF busy.
- The timestamp of a time 10 μs after the DGF starts acquiring after a T1 pulse.

In order to distinguish the two signals, they are combined using a linear fan-in/fan-out, but with one of them attenuated using a LEMO T-piece with a 50 Ω terminator.

The T1 timestamp is produced in a similar way to the proton supercycle timestamp. Both use the "10 μs after DGF not busy" signal, so the bottom three modules in figures 14 and 13 are the same.

17 Generation of the proton supercycle timestamp

We want to generate a DGF timestamp giving the time of arrival of the proton supercycle start signal and a time 10 μs after the first readout after a proton supercycle start signal.

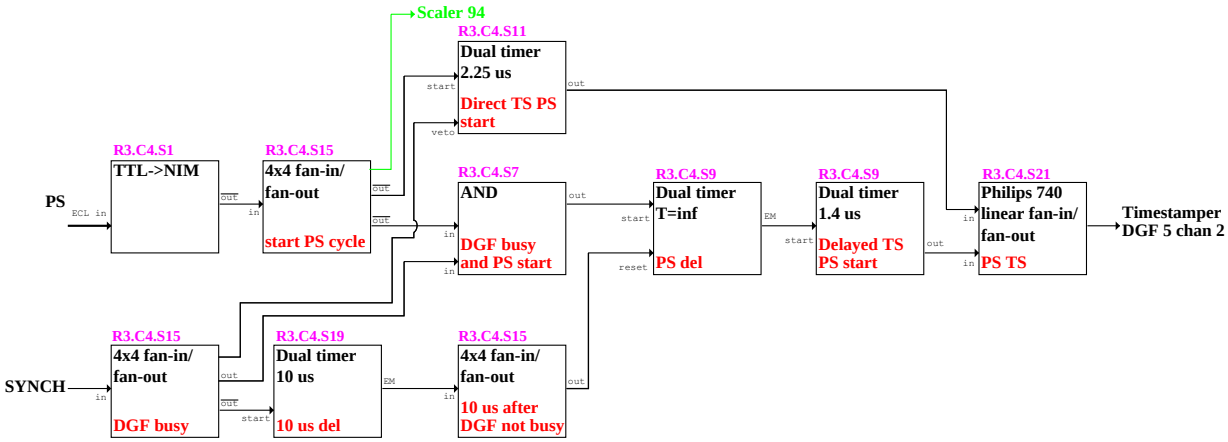

Figure 14: The generation of the proton supercycle timestamp

We receive an TTL signal each time that we get a proton supercycle start which we feed into an TTL → NIM converter. We do two things with this signal.

- Firstly, we use the signal to start a direct gate to indicate the start of the proton supercycle, which we send via a linear fan-in/fan-out to a timestamping DGF.
- Secondly, we want the timestamp for the first time the DGF is not busy after a supercycle start. To get this, we start a timer when the supercycle starts and the DGF is busy, and reset that timer 10 μs after the DGF is no longer busy. Then we use the end marker of that timer to generate a gate, which is sent to the same timestamping DGF via the linear fan-in/fan-out.

Note that the bottom three modules figures 14 and 13 are the same.

Why don't we attenuate one of the two inputs to the linear fan-in with a 50 Ω piece in order to get different pulse heights for the two kinds of signal? We do this with the T1 signal and it seems that we should do it to PS as well. I am told this isn't really that important for PS.

I notice that in May 2005, the inverted output from the TTL to NIM converter is being used. This must have already been like that in November 2004, but I'm not sure if it was like that in July 2004. My notes from July 2004 indicate we used the normal output, but this could be an error. In any case, now we use the inverted output.

18 Generation of the control signals for the scalers

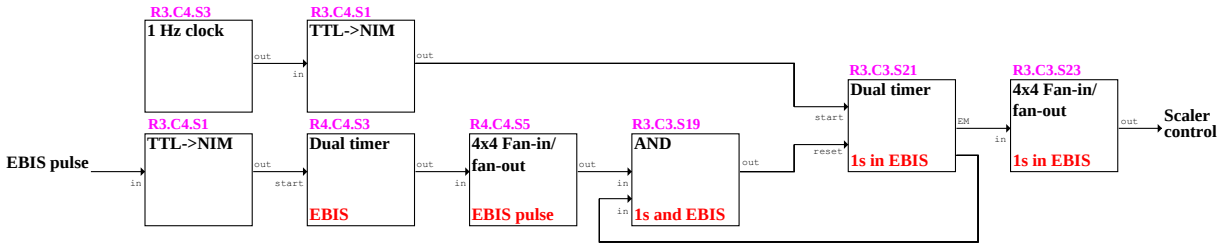

Figure 15: The generation of the control signals for the scalers

We want to read out the scalers every second. We convert a 1 Hz clock pulse into NIM and use it to start a gate which we fan out to the control inputs for the three scalers.

However, we only want to read when the EBIS pulse comes (on window), so we use the end marker of our gate and reset it with the EBIS pulse.

There was another change here between July and November 2004. An extra AND module was inserted between the fan-in/fan-out module called "EBIS pulse" and the reset for the "1 s in EBIS" dual timer. The other part of the and comes from the output of that dual timer, so the timer is only reset if it is actually running.

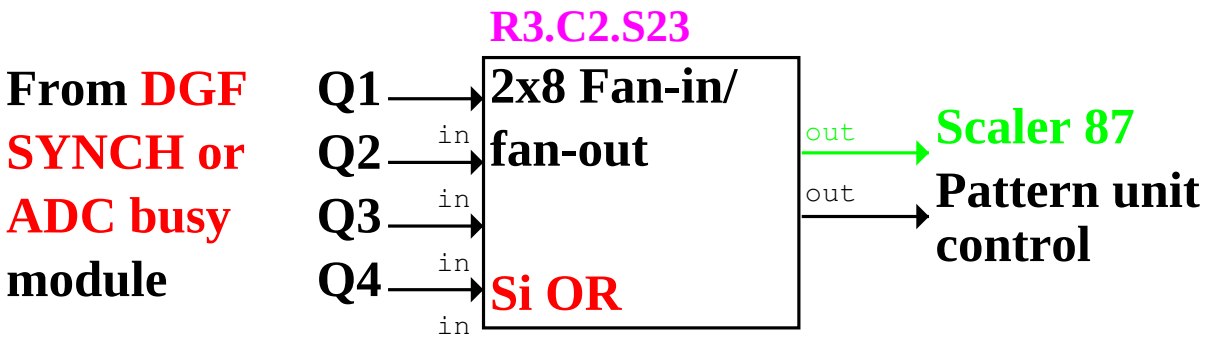

Figure 16: The generation of the control signals for the pattern unit. The four inputs come from the LeCroy 365 AND modules which generate the signal to produce the ADC gate for each quadrant, which is already vetoed by DAQ dead, ADC busy etc.

19 Generation of the control signals for the pattern unit

The pattern unit needs to record the pattern when each ADC gate occurs. However, we only have one pattern unit and four separate ADC gates (one for each quadrant) so we need to OR these signals logically. We take the signal out of the AND "DGF SYNCH or ADC busy" in the middle of figure 7 for each quadrant and pass them into a fan-in/fan-out. The resulting signal is the control for the pattern unit.

Note that the pattern unit needs a signal of at least 50 ns. This width is set in the "DGF SYNCH or ADC busy" modules (R3.C2.S13/15).

20 Generation of the forced readout

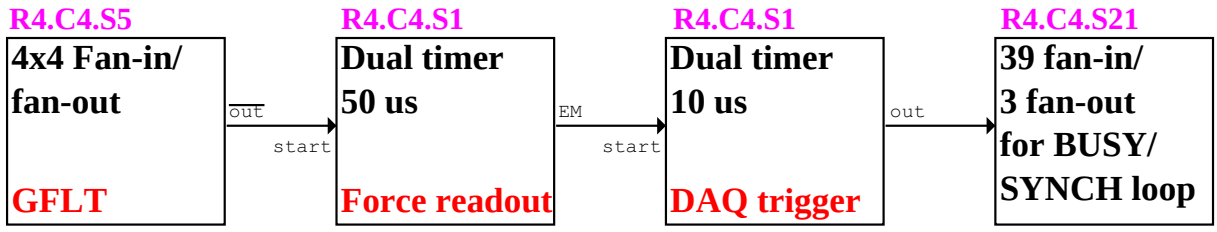

Figure 17: The generation of the forced readout

We take the GFLT signal, delay it 50 μs and then use it to generate a 10 μs wide pulse which we send to the fan-in of the DGF BUSY/SYNCH loop (see section 14). This causes the DGFs to finish their run and since the SYNCH is used to generate the DAQ trigger (see section 8).

Note that in 2004-5, the electronics for this were in rack 3, but they were moved to rack 4 in May 2006 in order to optimise the cables better.

21 The pattern unit bits

The first eight bits of the pattern unit correspond to the eight channels of the trigger box. i.e. downscaled quadrant 1, quadrant 1 and γ, downscaled quadrant 2 ...

In August 2004, we added in the laser on/off signal (bit 9) into the pattern unit. Note that this bit indicates the request that we send to the laser cabin (which is ignored in manual mode) not the actual state of the shutter.

Note that the highest bits should not be used as they are used internally in the acquisition program.

Bit	Signal
1	downscaled quadrant 1
2	quadrant 1 particle γ
3	downscaled quadrant 2
4	quadrant 2 particle γ
5	downscaled quadrant 3
6	quadrant 3 particle γ
7	downscaled quadrant 4
8	quadrant 4 particle γ
9	Laser on

22 Laser on/off

The laser on/off signal is generated from the PS signal, because we want to synchronise with a proton supercycle. The idea is to switch alternately one supercycle laser on, one supercycle with laser off.

In 2003 and 2004, a TTL signal was sent to the laser cabin and used to switch the laser on and off. The box in the laser cabin had a switch "TTL/MAN" which in TTL mode responded to this signal and in MAN mode remained either continuously open or closed according to the state of a second switch (which we left always "open"). The same signal which was sent as TTL to the laser cabin was sent as ECL to the pattern unit. The problem with this is that this means the acquisition records the state that the laser shutter should be in if set to TTL mode. However, if the switch is set to manual, the pattern unit still sees the alternating on/off cycle, even though the shutter is not moving. Furthermore, in 2004 we had the situation where the shutter itself jammed and then the acquisition recorded the state the shutter should have been in, not the actual state.

Another shortcoming of the setup in 2004 was the use of a timer to determine the length of time the shutter should stay open or closed. In fact, the supercycle length varies depending on the number of pulses per supercycle. Also, we don't know if the time between the arrival of the PS signal and the opening of the shutter is short enough if we get the first pulse in the supercycle. It is possible that the laser shutter isn't open fast enough, so that the first pulse is effectively in laser off mode, even though the bit says we are in laser on mode. This is not a problem if somebody else gets the first pulse and we get later ones.

In May 2005 a new system was installed. Now the PS signal is sent directly to some electronics in the laser cabin which does the switching automatically. This electronics is controlled by a control box in R2.C3.S13, to which it is connected by three cables. Depending on the position of the control on this module, the electronics in the laser cabin either sets "laser on", "laser off" or "laser on/off" (i.e. switching at each supercycle) modes. This means we don't have to go to the laser cabin in order to switch between laser on and laser on/off modes.

In addition, there is the laser status signal, which indicates the status of the shutter measured using an optical sensor. In 2005 this was a TTL signal which went through the TTL to NIM converter in R3.C4.S1 and from there up to the pattern unit. In 2006, it was a NIM signal which went directly from the laser cabin, via the control room and the patch panel on the wall into the pattern unit.

23 1 MHz and EBIS, 1 MHz and GFLT

For some reason these signals weren't documented in 2004. We simply take the logical AND of the 1 MHz clock signal (after conversion from TTL to NIM) and the EBIS signal. Since the EBIS signal is equivalent to the on window, this counts the number of microseconds in the on window. This result is sent to scaler 91. Similarly, we take the AND of the 1 MHz clock and the GFLT, which is equivalent to the on/off window and send it to scaler 92.

This means that we use scaler 90 to measure the time between scaler readouts in microseconds, scaler 91 to give the amount of time the on window was active in that period and scaler 92 gives the sum of the on window and the off window.

24 Ionisation chamber

In August 2004, the Munich people installed an ionisation chamber on another beamline sharing electronics with the rest of the Miniball DAQ. Its electronics is fairly simple. A signal is fed into a TFA, then a CFD and then ANDed with the inverted DAQ dead (i.e. DAQ not dead). This signal is passed into a gate generator and used to gate an ADC. The energy signals are sent into linear amplifiers and then into that ADC via a LEMO to flat cable converter.

We take the inverted out signal from the gate generator used to generate the ADC gate and send it to the coincidence unit in R3.C2.S15 labelled "DAQ trig if DAQ not busy" and and it with the other signals,

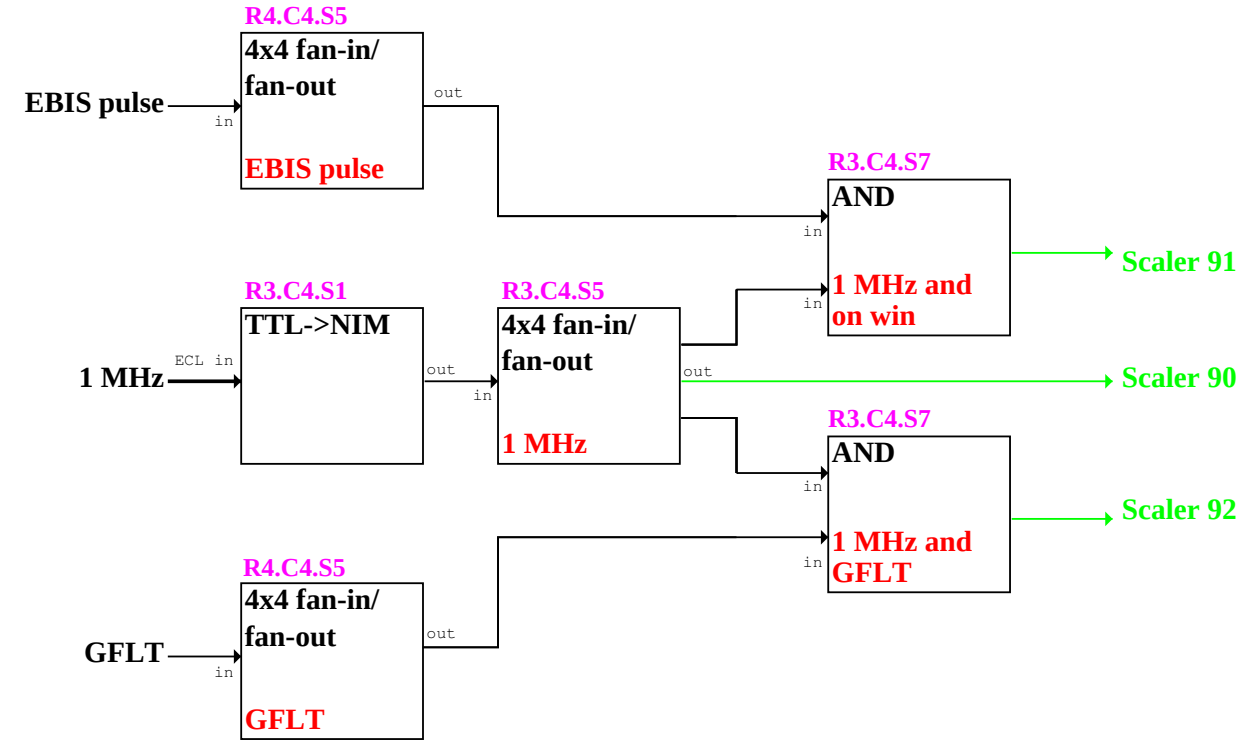

Figure 18: The 1 MHz signals.

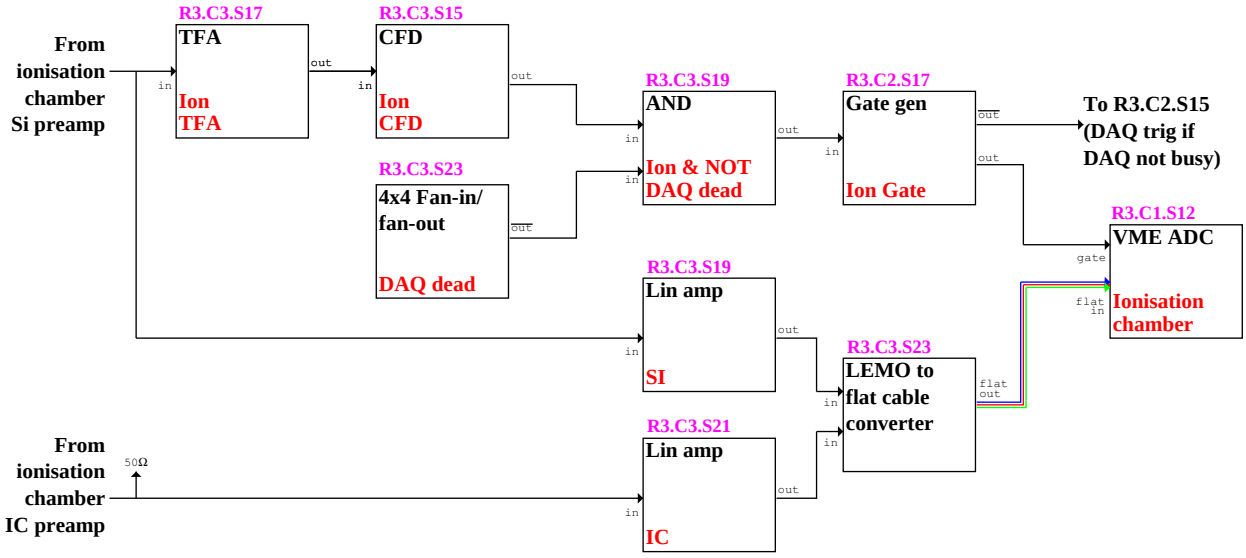

Figure 19: The electronics for the ionisation chamber.

removing the condition on the DGF SYNCH. This change can be made by pressing the buttons on the module. We remove the condition on the SYNCH and add the one on the ionisation chamber when we want to use the ionisation chamber and the other way round for normal operation. This is shown by a dashed line in figure 6.

Note that this electronics is used with a separate version of the DAQ, but it is set so that we just have to switch from one program to another without changing the electronics, other than pressing the two buttons on the coincidence unit mentioned in the previous paragraph.

In May 2005, a minor change was made, moving the ionisation chamber electronics from R2.C3 to R1.C3 and then in May 2006 they were moved back.

25 DGF backplane bus

The DGFs need to have a common 40 MHz clock shared by all modules, which is connected via the backplane bus. This is generated by one of the CAMAC 40 MHz clock modules, which is set to master. Never connect

an input to a module set to master. The output of the master goes to the input of another clock set to slave and its output goes to the input of a third module set to slave etc. These connections are made with IEEE-1394 (Firewire) cables at the front.

At the back of these clock modules there are three outputs which can be used to fan out to up to eight DGFs per output. So one module is enough per crate. A flat cable is used to connect each DGF to the clock with an adaptor piece at one end and a terminator piece at the other.

The DGF has two triggers: a fast trigger sent as soon as an event is detected and a slow DSP trigger sent after the slow filter time (i.e. about 10 μs later. These are available on the same backplane bus as the 40 MHz clock. For Miniball, we have seven signals per capsule on two DGFs, and only the core is allowed to generate a signal. So the trigger lines between those two DGFs need to be connected. Then the core channel can trigger the segments in the same DGF and those in the second DGF. The trigger lines between DGF modules with signals from different clusters should be cut. To do this, physically cut out the four middle wires of the 16 wire flat cable between modules that are not for the same capsule, but leave the other wires (clock etc.) present. Note, that for the special signals for the timestamping DGFs, these are all independent, so all the trigger wires should be cut there.

Unfortunately, because the DGF bus is incorrectly terminated, it was not possible to protect the driver IC of the clock module against misconnection. So if you connect up something wrongly, you will probably blow the AD8017 driver IC for that channel. Don't then swap the channels or you will kill another one!

26 Scalers

There are three 32-channel scaler modules in use. Scalers 1 to 64 are for the PPAC. The third has a variety of different signals from different sources.

Scaler	Signal	Scaler	Signal
65	Q1 free	73	Q1 accepted
66	Q2 free	74	Q2 accepted
67	Q3 free	75	Q3 accepted
68	Q4 free	76	Q4 accepted
69	Q1 delayed	77	Q1 and gamma
70	Q2 delayed	78	Q2 and gamma
71	Q3 delayed	79	Q3 and gamma
72	Q4 delayed	80	Q4 and gamma

Scaler	Signal	Scaler	Signal
81	Q1 gate	89	GFLT
82	Q2 gate	90	1 MHz
83	Q3 gate	91	1 MHz and on win
84	Q4 gate	92	1 MHz and GFLT
85	EBIS pulse	93	T1
86	Total DGF	94	PS
87	Si OR	95	
88	SYNCH	96	

27 Positions of modules in crates and racks

The racks are numbered from 1 to 5 with 1 being closest to the wall. The crates are numbered from 1 with crate 1 being highest. The notation R1.C2 means rack one crate two and R1.C2.S15 refers to the module in slot 15 of that crate. These numbers are shown on the circuit diagrams.

27.1 Rack 1

In rack 1 we have the PPAC HV supply and one camac crate without a crate controller.

27.1.1 CAMAC crate R1.C2

- Slot 17 - LeCroy 4532 MALU (Quadrant 1 OR)
- Slot 19 - LeCroy 4532 MALU (Quadrant 2 OR)
- Slot 21 - LeCroy 4532 MALU (Quadrant 3 OR)
- Slot 23 - LeCroy 4532 MALU (Quadrant 4 OR)

Figure 20: R1.C1: PPAC power supply. We normally use about +400 Volts

27.2 Rack 2

In rack 2 we have two crates for the RAL 109 modules with their power supplies and a low-power NIM crate.

27.2.1 KM-6 crate R2.C1

- Slot 1 - RAL 109 s/n 70 (annular strips)
- Slot 2 - RAL 109 s/n 71 (annular strips)
- Slot 3 - RAL 109 s/n 72 (annular strips)
- Slot 4 - RAL 109 s/n 73 (annular strips)
- Slot 5 - RAL 109 s/n 74 (annular strips)
- Slot 6 - RAL 109 s/n 75 (annular strips)
- Slot 7 - RAL 109 s/n 76 (annular strips)
- Slot 8 - RAL 109 s/n 77 (annular strips)
- Slot 12 - RAL 109 s/n 90 (PAD detector)
- Slot 13 - RAL 109 s/n 91 (unused)

27.2.2 KM-6 crate R2.C2

- Slot 1 - RAL 109 s/n 78 (sector strips)
- Slot 2 - RAL 109 s/n 79 (sector strips)
- Slot 3 - RAL 109 s/n 80 (sector strips)
- Slot 4 - RAL 109 s/n 81 (sector strips)

Figure 21: R1.C2: The cabling of MALUs - four multicoloured flat cables (one from each quadrant - the other ends are split in pairs, so they go to 8 RAL109s) come from the RAL109s in R2.C2 (i.e. the front rings) to the inputs. Four blue and white flat cables go from the outputs of the MALU to the TDCs. The ORO output of each MALU goes to the ECL→NIM converter (R2.C3.S1).

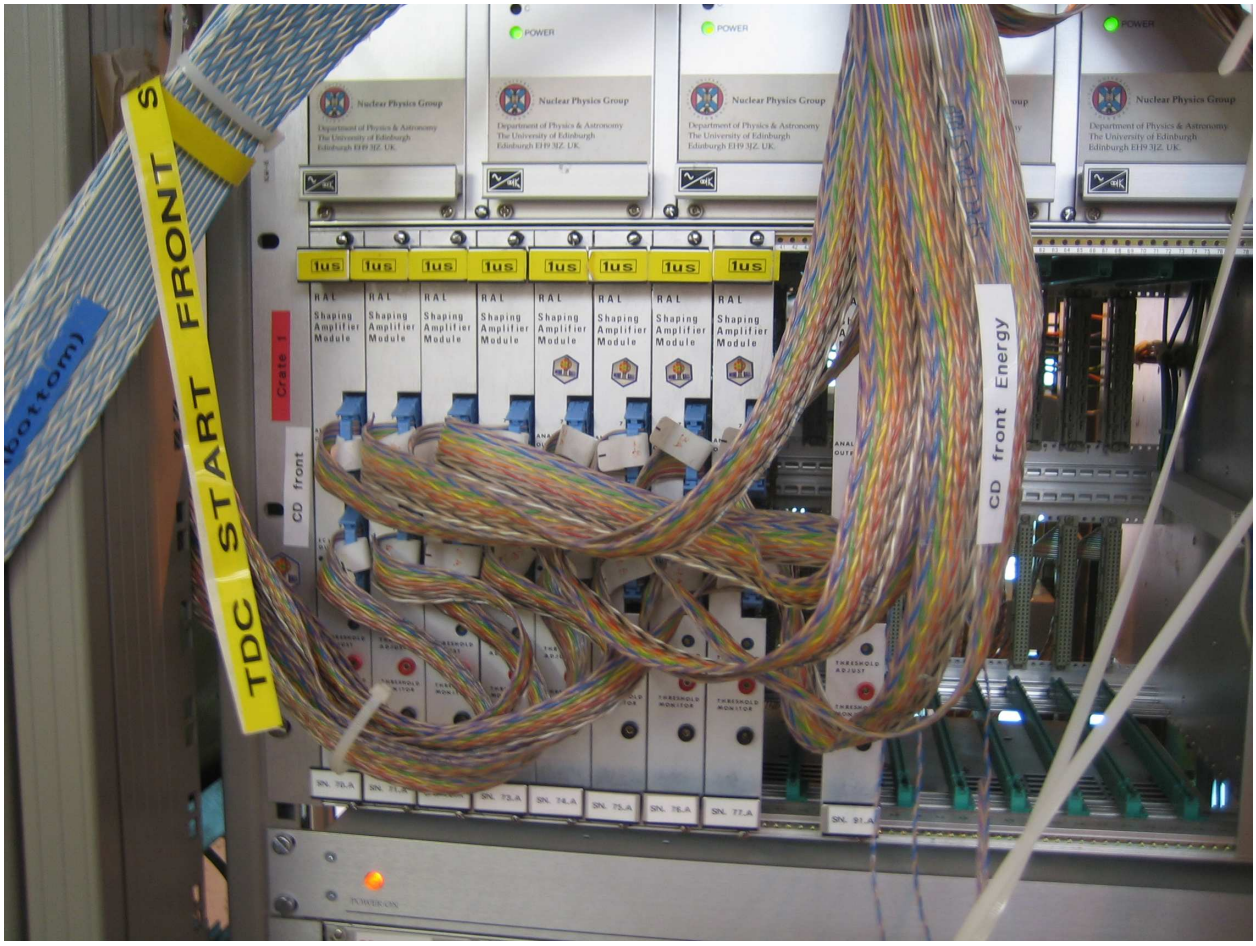

Figure 22: R2.C1: The RAL109s for the front rings. The upper connections are for the energy and they are joined up in pairs and sent to the ADC. The lower connections are for the timing and they go to the MALU in R1.C2 and from there to the TDCs in R3.C1.

- Slot 5 - RAL 109 s/n 82 (sector strips)
- Slot 6 - RAL 109 s/n 83 (sector strips)
- Slot 7 - RAL 109 s/n 84 (sector strips)
- Slot 8 - RAL 109 s/n 85 (sector strips)
- Slot 9 - RAL 109 s/n 86 (sector strips)
- Slot 10 - RAL 109 s/n 87 (sector strips)
- Slot 11 - RAL 109 s/n 88 (sector strips)
- Slot 12 - RAL 109 s/n 89 (sector strips)

27.2.3 NIM crate R2.C3

- Slot 1-2 ECL → NIM converter (particle trigger)
- Slot 3-4 Silena quad bias supply (CD E detector bias (not used))
- Slot 5-6 Silena quad bias supply (CD bias)
- Slot 7-8 Ortec 480 pulser (CD pulser)
- Slot 9-10 12 Volt power
- Slot 11-12 Triple preamp power supply “beam dump detector”, “ΔE 1”, “ΔE 2”
- Slot 13-14 Laser control box
- Slot 15-16 CF4000 quad CFD “unused”, “unused”, “ionisation chamber” “unused”
- Slot 17-18 Ortec 454 TFA “ionisation chamber”

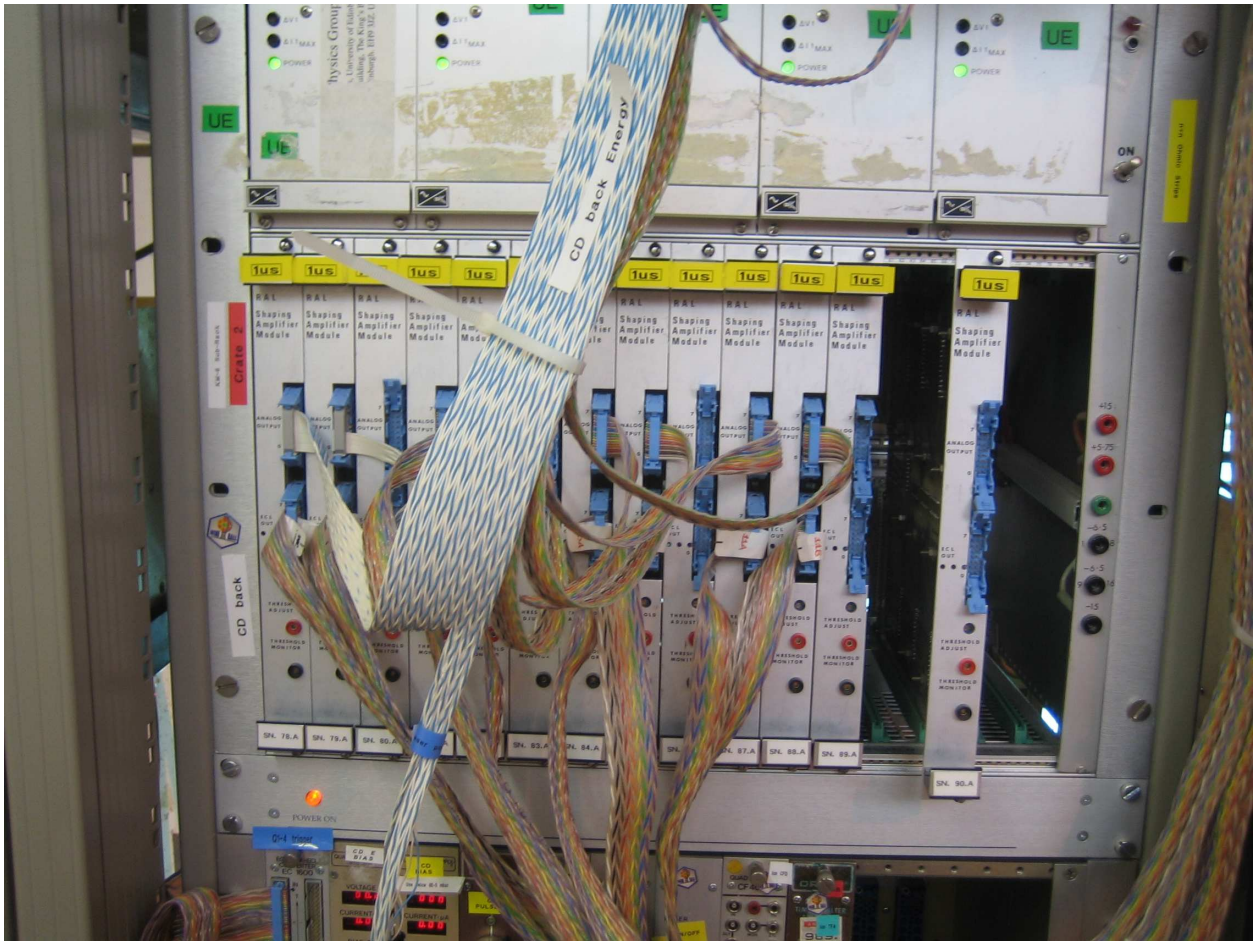

Figure 23: R2.C2: The RAL109s for the back sectors. The upper connections are for the energy and they are joined up in pairs and sent to the ADC. Note that the first pair has the blue and white cable on to which the signal for laser power is added. The lower connections are for the timing and they go directly to the TDC in R3.C1

27.3 Rack 3

In rack 3 we have a VME crate and three high-power NIM crates.

27.3.1 VME crate R3.C1

- Slot 1 - power PC
- Slot 2 - VME trigger module
- Slot 4 - CAEN V785 AG ADC
- Slot 5 - CAEN V785 AG ADC
- Slot 6 - CAEN V785 AG ADC
- Slot 7 - CAEN V785 AG ADC
- Slot 8 - CAEN V775 TDC
- Slot 9 - CAEN V775 TDC
- Slot 10 - CAEN V775 TDC
- Slot 11 - CAEN V775 TDC
- Slot 12 - CAEN V785 AG ADC (for ionisation chamber)
- Slot 13 - pattern unit
- Slot 14 - scaler with NIM inputs

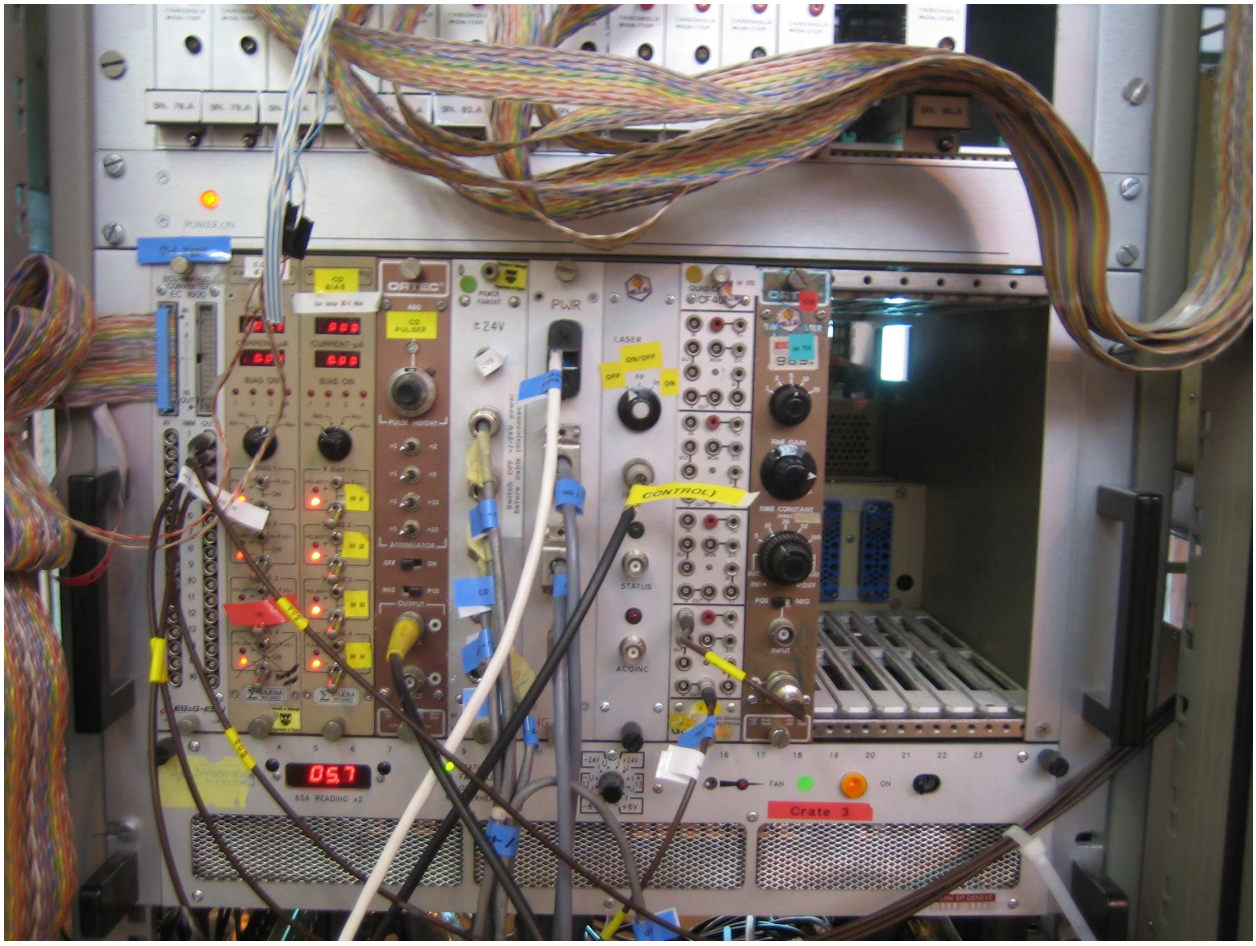

Figure 24: R2.C3: NIM crate - various modules for CD power, laser etc.

- Slot 15 - scaler with ECL inputs (PPAC Y)
- Slot 16 - scaler with ECL inputs (PPAC X)
- Slot 17 - Wiener VC32
- Slot 18 - Wiener VC32
- Slot 19 - Wiener VC32
- Slot 20 - Wiener VC32 (not used)
- Slot 21 - VDIS

27.3.2 NIM crate R3.C2

- Slot 1-6 - TB8000 trigger box (triple width) “Trigger box”
- Slot 7-8 - CAEN N454 4x4 fan-in/fan-out “Delay trg Q1...4”
- Slot 9-10 - LeCroy 370C strobed coinc “coinc PG1...4”, “four channels unused”
- Slot 11-12 - CAEN N455 quad coinc logic “Q1...4 coinc or downscaled”
- Slot 13-14 - LeCroy 465 triple coinc unit “DGF Synch or ADC busy for Q1...3”
- Slot 15-16 - LeCroy 465 triple coinc unit “DGF Synch or ADC busy for Q4”, “DAQ trig if DAQ not busy”, “unused”
- Slot 17-18 - GG8000 octal gate generator “Q1...4 ADC/TDC gate”, “Ion gate”, “Bad”, “DAQ trigger”, “γ OR”
- Slot 19-20 - LeCroy 429A 4x4 fan-in/fan-out “Q1...4 ADC/TDC gate”
- Slot 21-22 - IKP modified TFA (in Ortec housing) “Mult out”
- Slot 23-24 - CAEN N454 2x8 fan-in/fan-out “Gamma Or”, “Si OR”

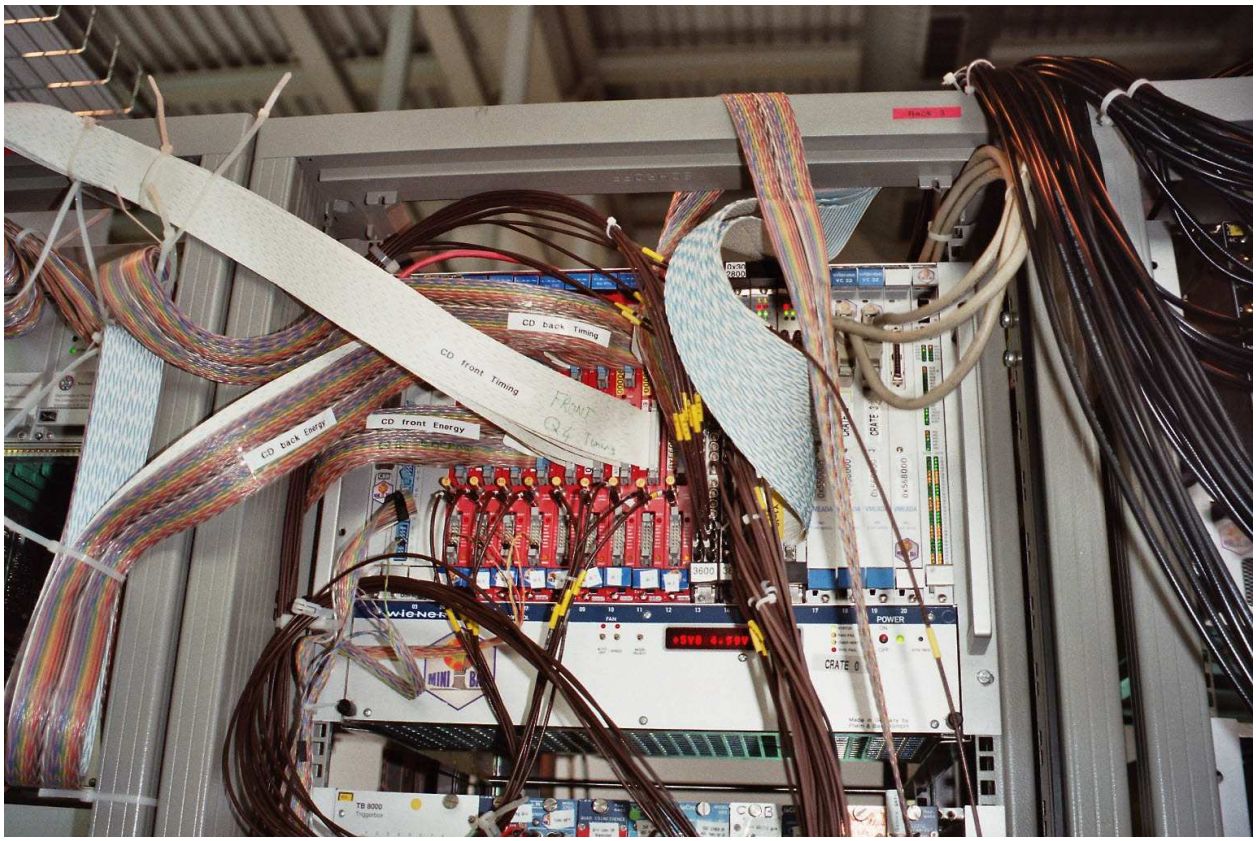

Figure 25: R1.C3: The cabling of the CD to the VME ADCs and TDCs. The four ADCs are the left red modules and the four TDCs are the next four. The front signals use the lower parts of the ADCs and TDCs and the back signals use the upper parts. Also shown is the bunch of LEMO cables for the scalers, the pair of blue and white flat cables for the PPAC and the SCSI cables for the VC32→CC32 connection

27.3.3 NIM crate R3.C3

- Slot 1-2 - TTL/NIM → ECL converter (set to NIM) “DAQ Trigger”
- Slot 3-4 - ECL → TTL/NIM converter (set to NIM) “DAQ dead”, “ADC dead”
- Slot 5-6 - LeCroy 429A 4x4 fan-in/fan-out “ADC 1 busy”, “ADC 2 busy”, “ADC 3 busy”, “ADC 4 busy”
- Slot 7-8 - Noname dual timer “Delay Q1 (both parts)”
- Slot 9-10 - CAEN N93B dual timer “Delay Q2 (both parts)”
- Slot 11-12 - Noname dual timer “Delay Q3 (both parts)”
- Slot 13-14 - CAEN N93B dual timer “Delay Q4 (both parts)”
- Slot 15-16 - LeCroy 429A 4x4 fan-in/fan-out “Q1. . . 4 trigger”
- Slot 17-18 - Empty slot
- Slot 19-20 - LeCroy 465 triple coincidence unit “unused”, Ion and not DAQ dead”, “1s and EBIS”
- Slot 21-22 - CAEN 2255A Dual Timer “DAQ dead extend”, “1s in EBIS”
- Slot 23-24 - CAEN N454 4x4 fan-in/fan-out “DAQ dead”, “DAQ dead+”, “DAQ dead+”, “1s in EBIS”

27.3.4 NIM crate R3.C4

- Slot 1-2 - TTL → NIM and NIM → TTL converter “EBIS pulse”, “PS”, “T1”
- Slot 3-4 - Clock “1 Hz”, “1 MHz”
- Slot 5-6 - LeCroy 429A 4x4 fan-in/fan-out “not used”, “1 MHz”, “not used”, “not used”

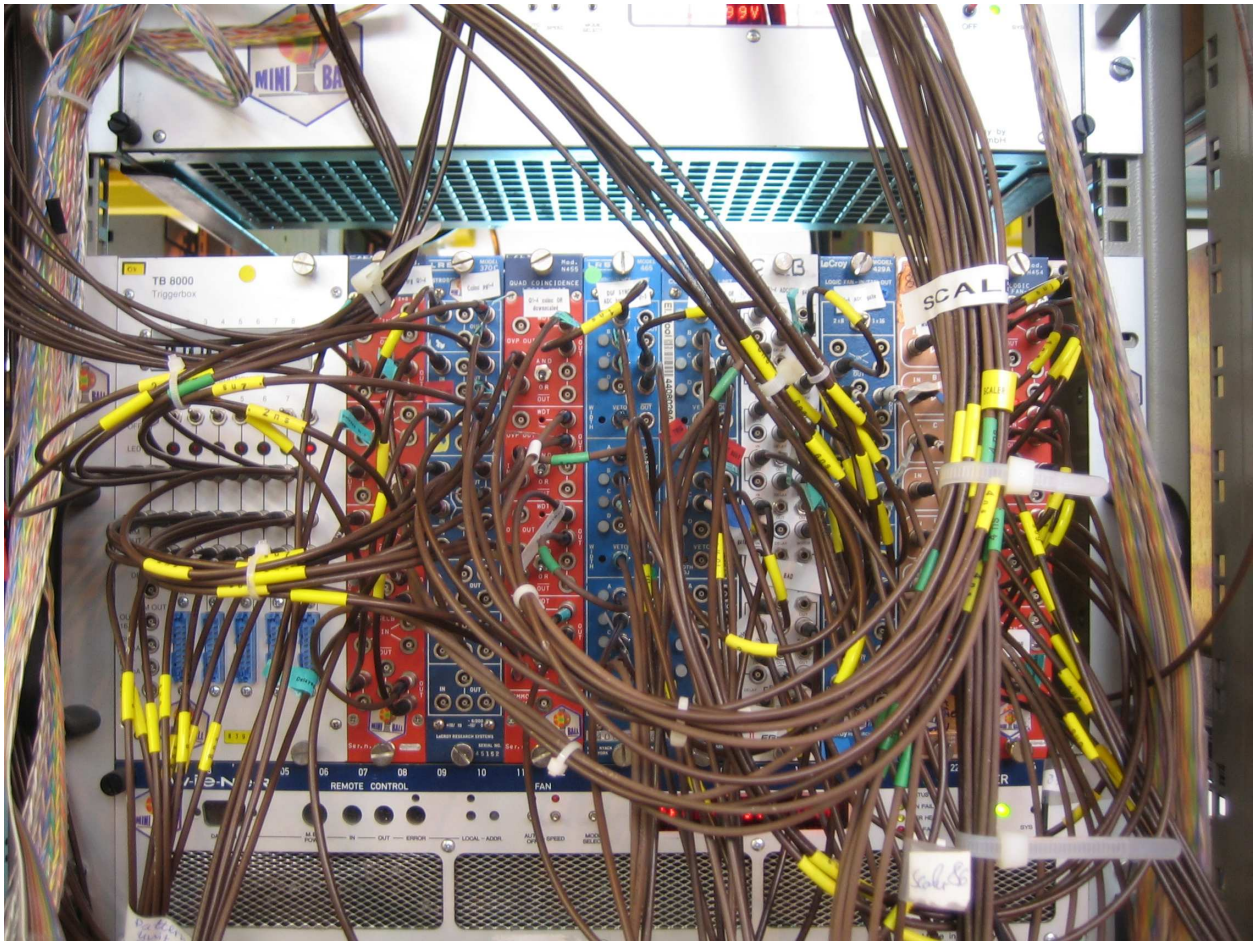

Figure 26: R3.C2: NIM crate - mostly trigger logic

- Slot 7-8 - CAEN N455 quad coinc logic "T1 AND DGF busy", "1 MHz and on win", "1 MHz and GFLT", "DGF busy and PS start"
- Slot 9-10 - Noname dual timer "Delayed TS PS start", "PS del"
- Slot 11-12 - CAEN 2255B dual timer "unused", "direct TS PS start"
- Slot 13-14 - Empty slot
- Slot 15-16 - CAEN N454 4x4 fan-in/fan-out "T1", "start PS cycle", "DGF busy", "10 μs after DGF not busy"
- Slot 17-18 - CAEN N93B dual timer "T1 veto", "TS delay"
- Slot 19-20 - CAEN 2255B dual timer "10 μs del", "unused"
- Slot 21-22 - Philips quad linear fan-in/fan-out "PS TS", "T1 not busy"
- Slot 23-24 - CAEN 2255B dual timer "TS gate T1", "TS gate T1 delay"

27.4 Rack 4

In rack 4 we have three CAMAC crates and one high-power NIM crate.

27.4.1 CAMAC crate R4.C1

- Slot 3 - XIA DGF 1154
- Slot 4 - XIA DGF 1153
- Slot 5 - XIA DGF 1119
- Slot 6 - XIA DGF 1103

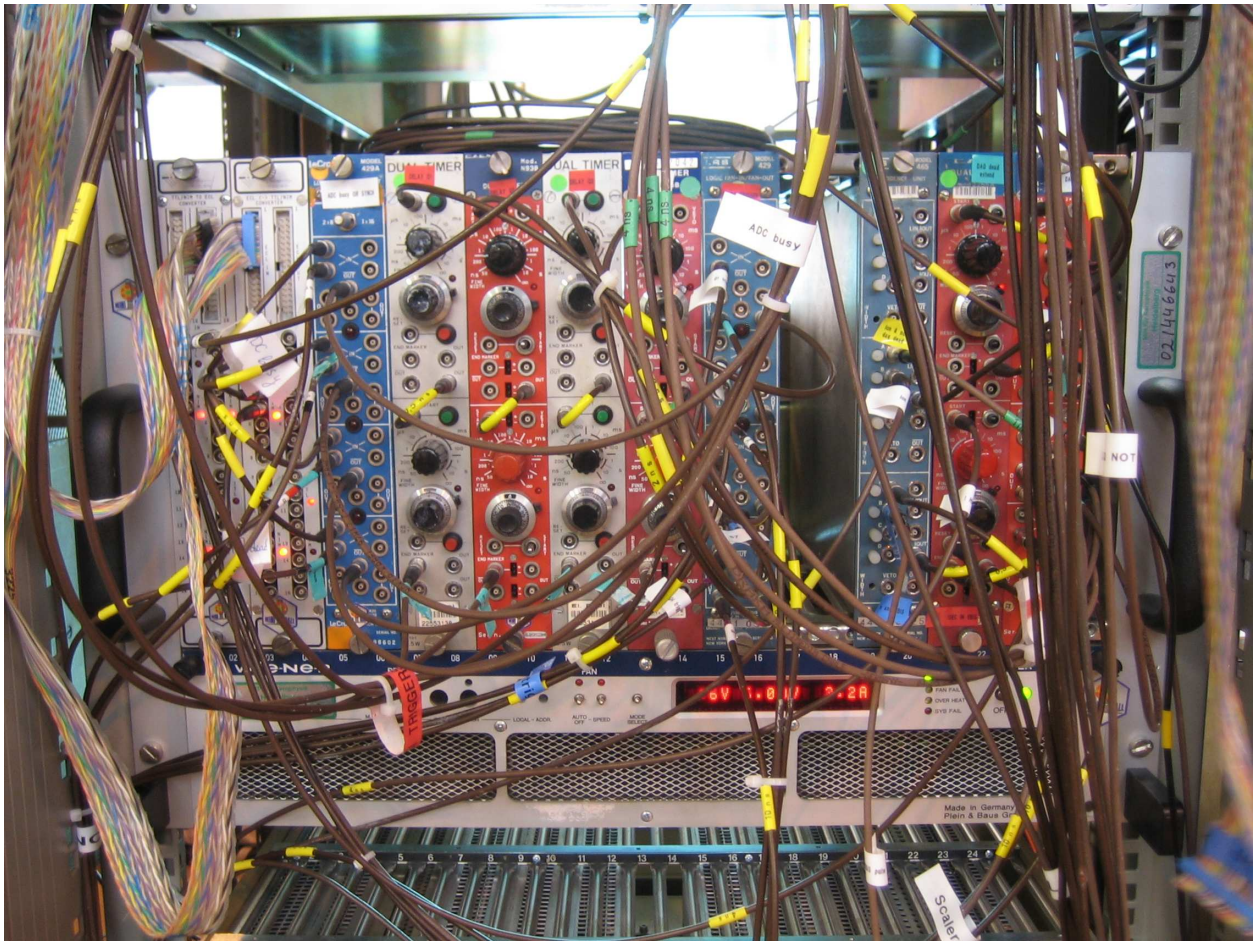

Figure 27: R3.C3: NIM crate - mostly trigger logic

- Slot 7 - XIA DGF 1101
- Slot 8 - XIA DGF 1148
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1158
- Slot 11 - XIA DGF 1107
- Slot 12 - XIA DGF 1163
- Slot 13 - XIA DGF 1139
- Slot 14 - XIA DGF 1162
- Slot 15 - XIA DGF 1161
- Slot 16 - XIA DGF 1120
- Slot 17 - XIA DGF 1166
- Slot 18 - XIA DGF 1194
- Slot 19 - XIA DGF 1184
- Slot 20 - XIA DGF 1122
- Slot 21 - XIA DGF 1174
- Slot 24-25 Wiener CC32

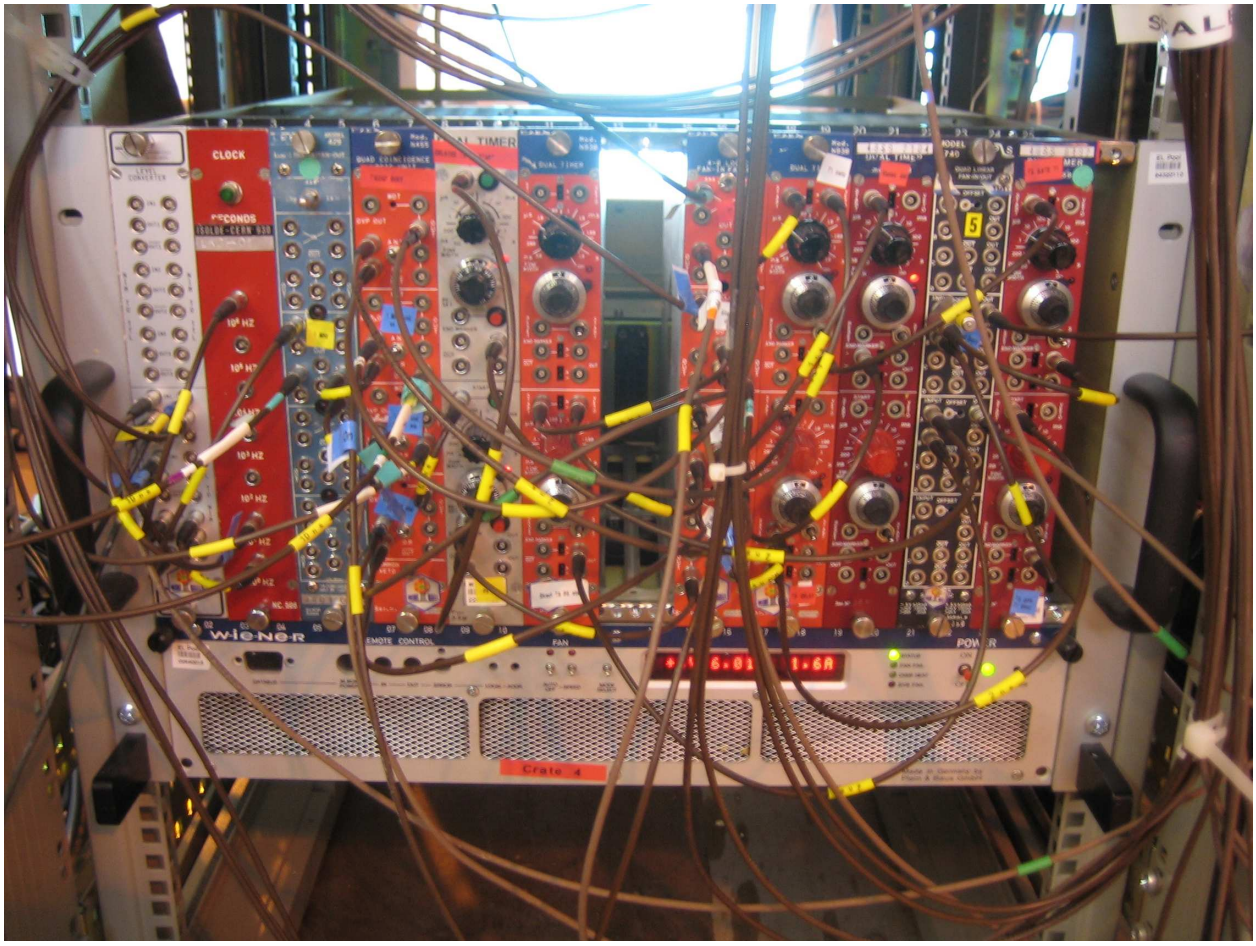

Figure 28: R3.C4: NIM crate - mostly PS and T1 signals

27.4.2 CAMAC crate R4.C2

- Slot 3 - XIA DGF 1176
- Slot 4 - XIA DGF 1175
- Slot 5 - XIA DGF 1159
- Slot 6 - XIA DGF 1171
- Slot 7 - XIA DGF 1106
- Slot 8 - XIA DGF 1100
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1108
- Slot 11 - XIA DGF 1190
- Slot 12 - XIA DGF 1152
- Slot 13 - XIA DGF 1167
- Slot 14 - XIA DGF 1113
- Slot 15 - XIA DGF 1104
- Slot 16 - XIA DGF 1130
- Slot 17 - XIA DGF 1123
- Slot 18 - XIA DGF 1192
- Slot 19 - XIA DGF 1138

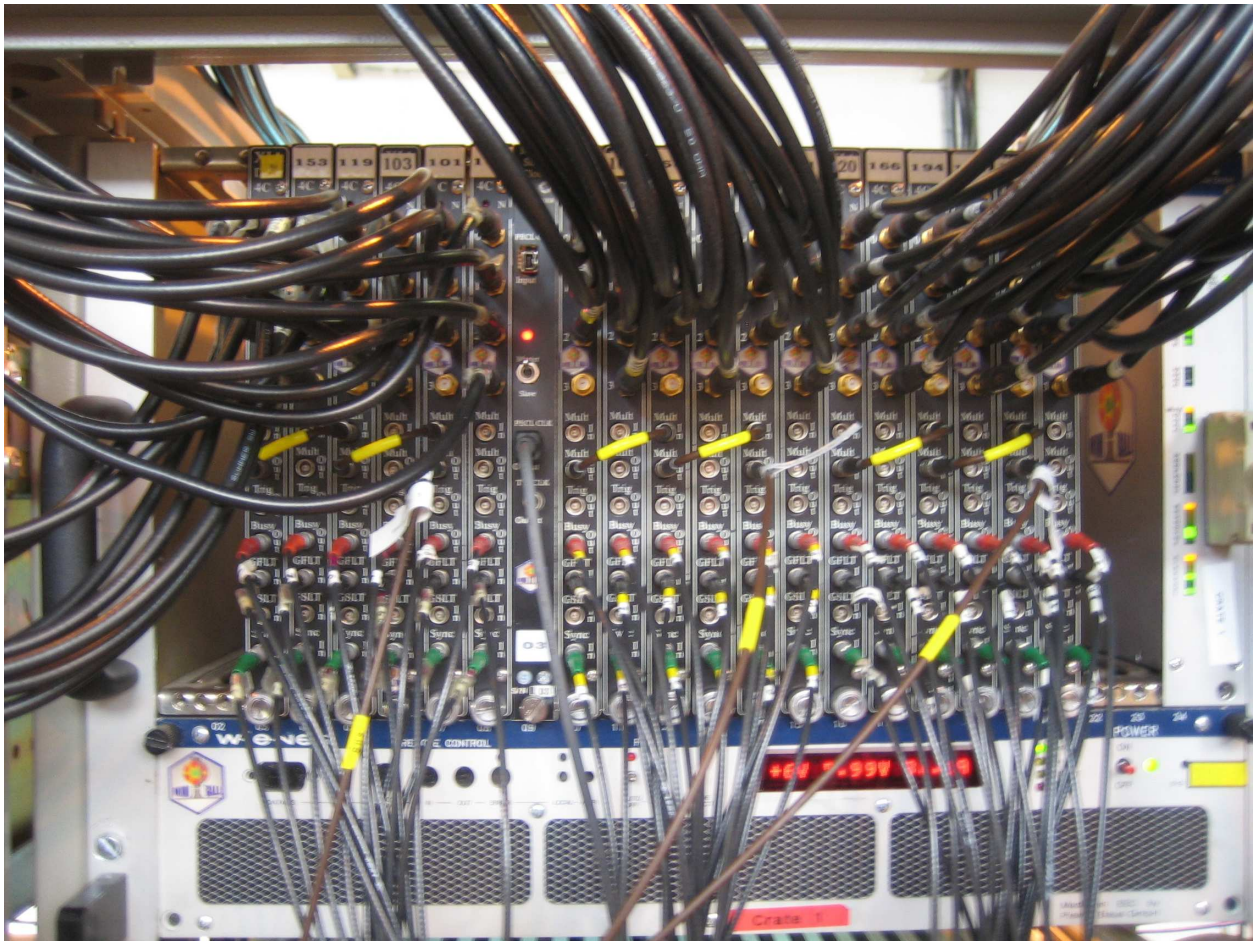

Figure 29: R4.C1: CAMAC crate of DGFs for three clusters.

- Slot 20 - XIA DGF 1128
- Slot 21 - XIA DGF 1147
- Slot 24-25 Wiener CC32

27.4.3 R4.C3

- Slot 4 - XIA DGF 1132 “Q1 timestamp”
- Slot 5 - XIA DGF 1178 “Q2 timestamp”
- Slot 6 - XIA DGF 1149 “Q3 timestamp”
- Slot 7 - XIA DGF 1137 “Q4 timestamp”
- Slot 8 - XIA DGF 1142 “EBIS”, “T1”,”PS”
- Slot 9 - XIA DGF 1189 “Beam dump”, “ΔE1”,“ΔE2”
- Slot 10 - IKP 40 MHz clock
- Slot 11 - XIA DGF 1124
- Slot 12 - XIA DGF 1170
- Slot 13 - XIA DGF 1169
- Slot 14 - XIA DGF 1129
- Slot 15 - XIA DGF 1151
- Slot 16 - XIA DGF 1150
- Slot 17 - XIA DGF 1145

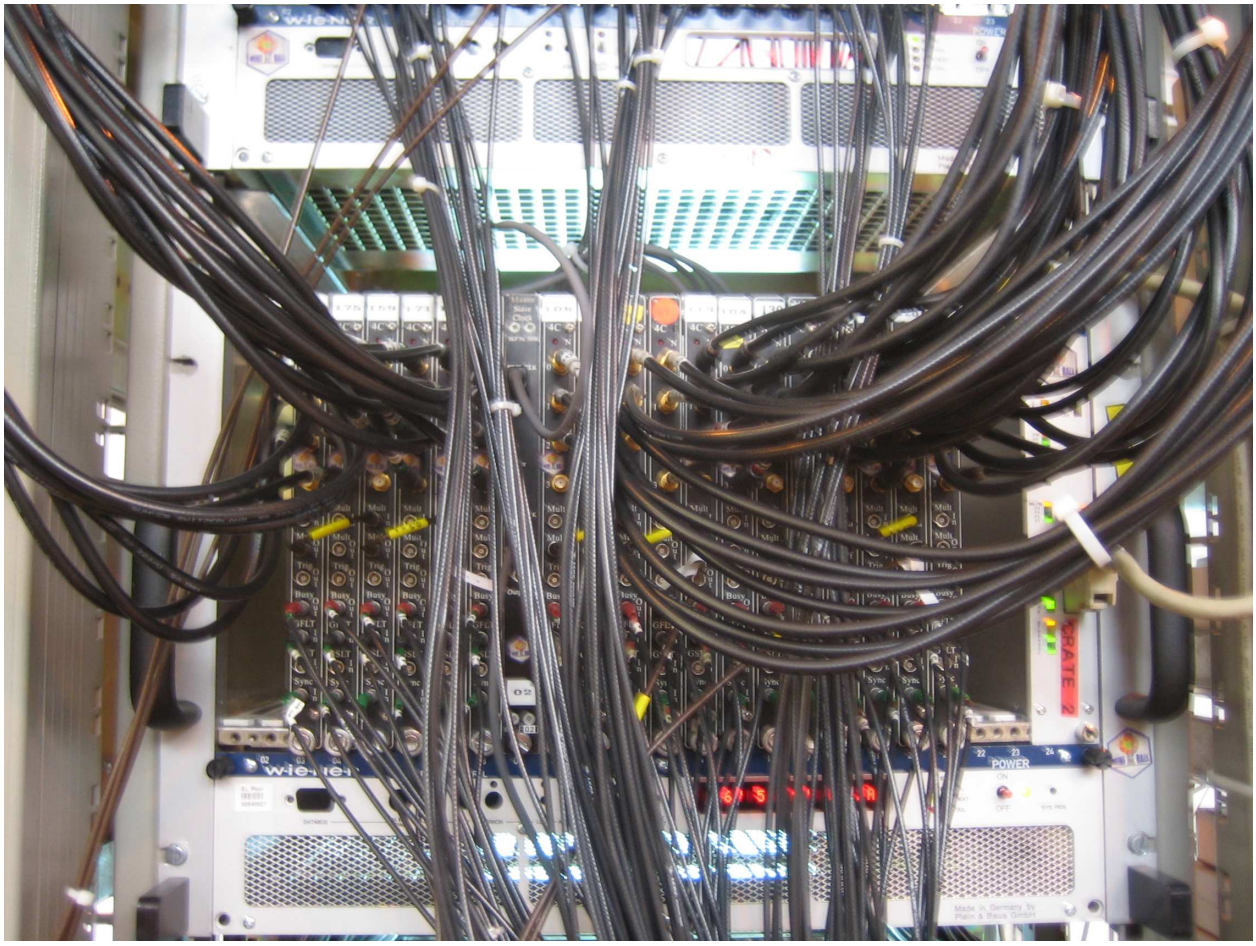

Figure 30: R4.C2: CAMAC crate of DGFs for three clusters.

- Slot 18 - XIA DGF 1118
- Slot 19 - XIA DGF 1134
- Slot 20 - XIA DGF 1193
- Slot 21 - XIA DGF 1188
- Slot 22 - XIA DGF 1109
- Slot 24-25 Wiener CC32

27.4.4 NIM crate R4.C4

- 1-2 - CAEN N93B dual timer "Force readout", "DAQ trigger"
- 3-4 - CAEN N93B dual timer "EBIS", "Max on/off window"
- 5-6 - CAEN N454 4x4 fan-in/fan-out "EBIS pulse", "EBIS pulse", "GFLT", "not used"
- 7-8 - LeCroy 365AL 4-fold logic unit "unused", "End RDO and in time"
- 9-10 - CAEN N93B dual timer "TDGF Ebis", "Off window"
- 11-12 - CAEN 2255B dual timer "Not busy", "End RDO"
- 13-14 - IKP 3 fan-in/39 fan-out "GFLT"
- 15-16 - IKP 3 fan-in/39 fan-out "GFLT"
- 17-18 - IKP 3 fan-in/39 fan-out "Synch"
- 19-20 - IKP 3 fan-in/39 fan-out "Synch"
- 21-22 - IKP 39 fan-in/3 fan-out "Busy"
- 23-24 - IKP 39 fan-in/3 fan-out "Busy"

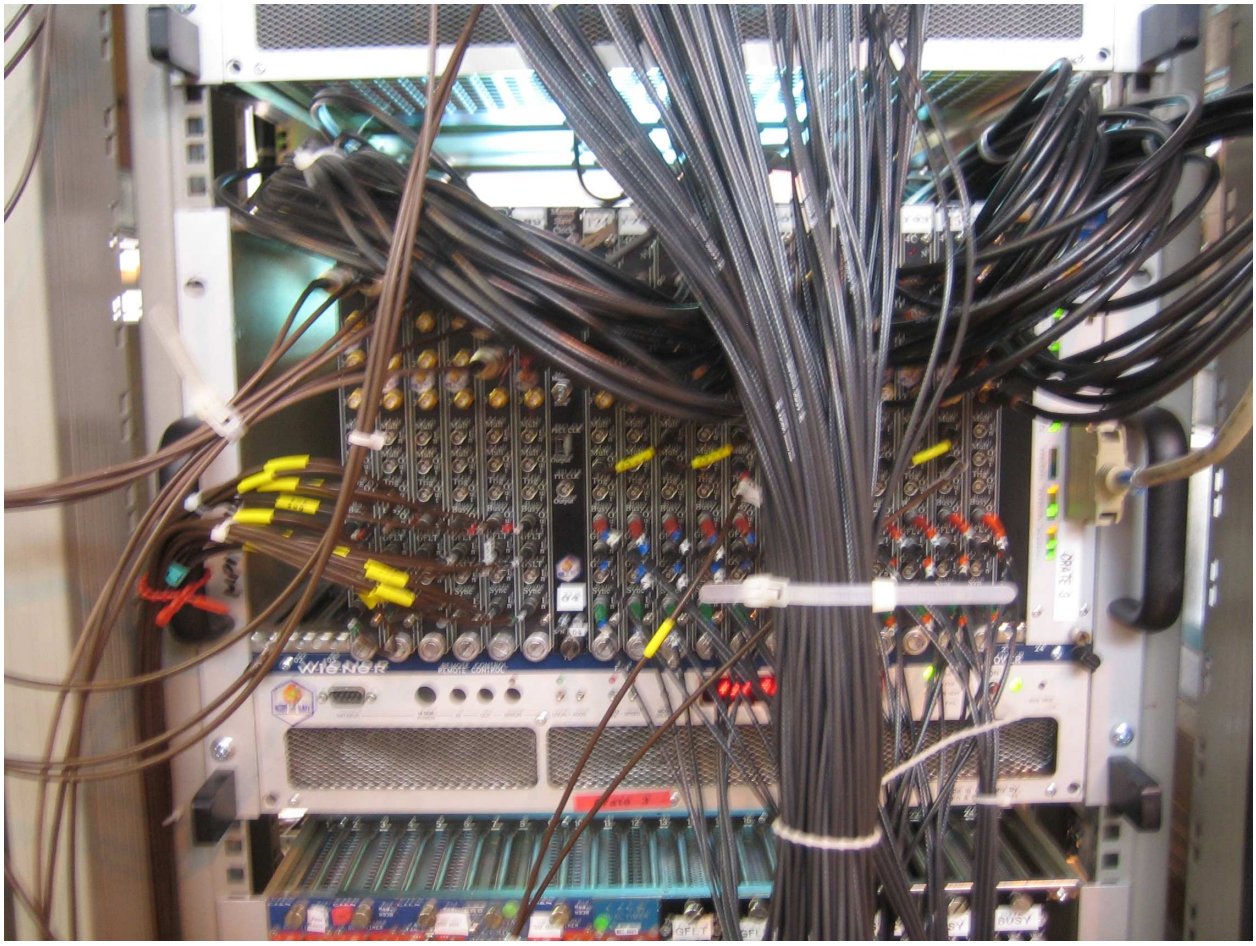

Figure 31: R4.C3: CAMAC crate of DGFs. Note the left four are the timestamper DGFs, then there is the EBIS etc. DGF and the sixth DGF is for the beam dump detector.

27.5 Rack 5

Rack five contains (from top to bottom) the filling computer monitor, the filling computer, its keyboard, the PT100 box, the four manifold controller boxes (with box D highest), raid array, DAQ computer, UPS and CAEN HV power supply.

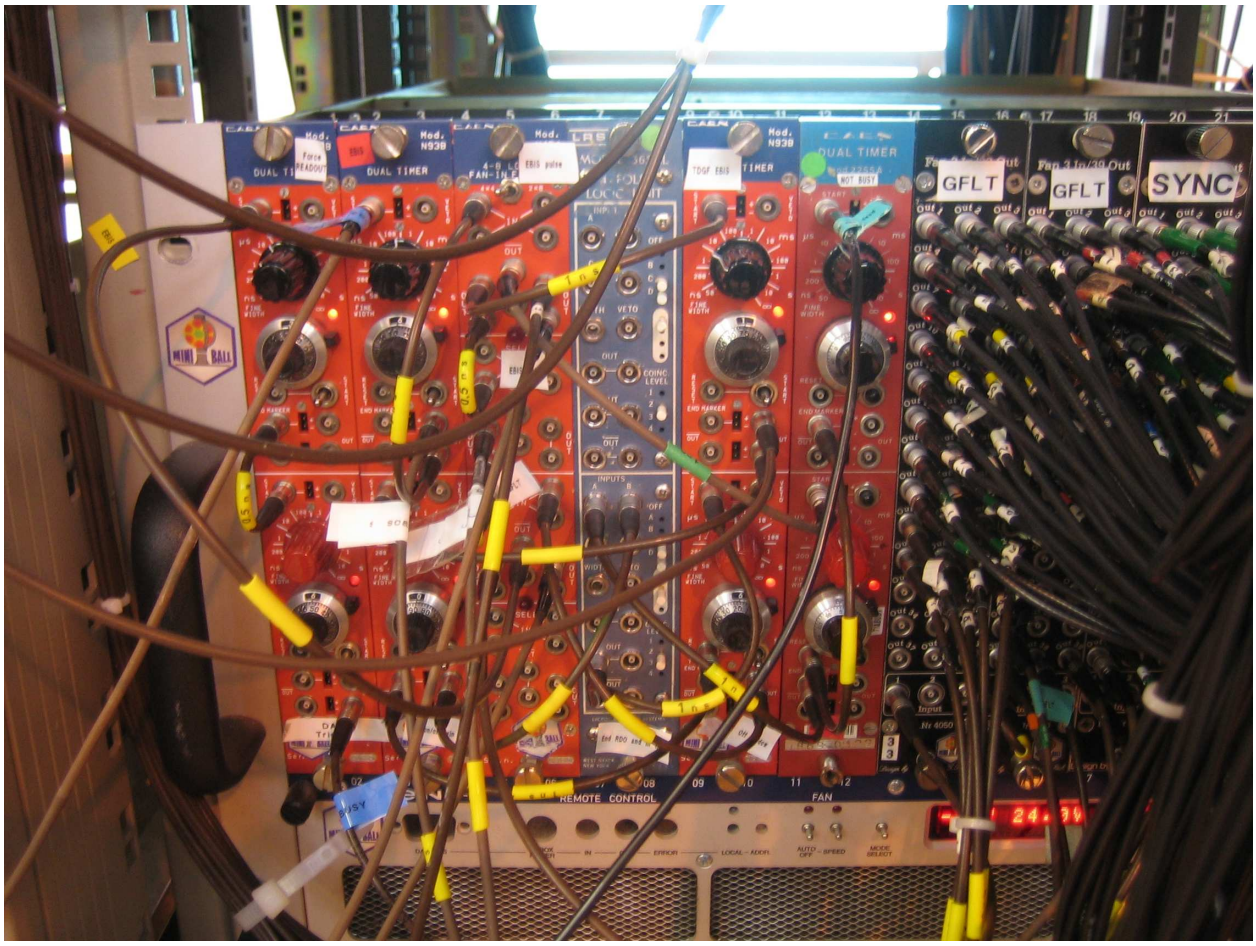

Figure 32: R4.C4: NIM crate

Figure 33: R5 top: filling system computer with monitor and keyboard, PT100 box and four manifold controller boxes.

Figure 34: R5 bottom: Raid array, DAQ computer, UPS, CAEN HV power supply.