Miniball electronics at May 2010

Contents

[1] Nigel Warr 31 May 2010

1 Foreword

This document describes the state of the electronics used at CERN for the May 2010 setup. It is based on the one for It is based on the one for May 2008, which was based on the one for June 2007, which was based on the one for May 2006, which was based on May 2005, which in turn was based on the one for July 2004.

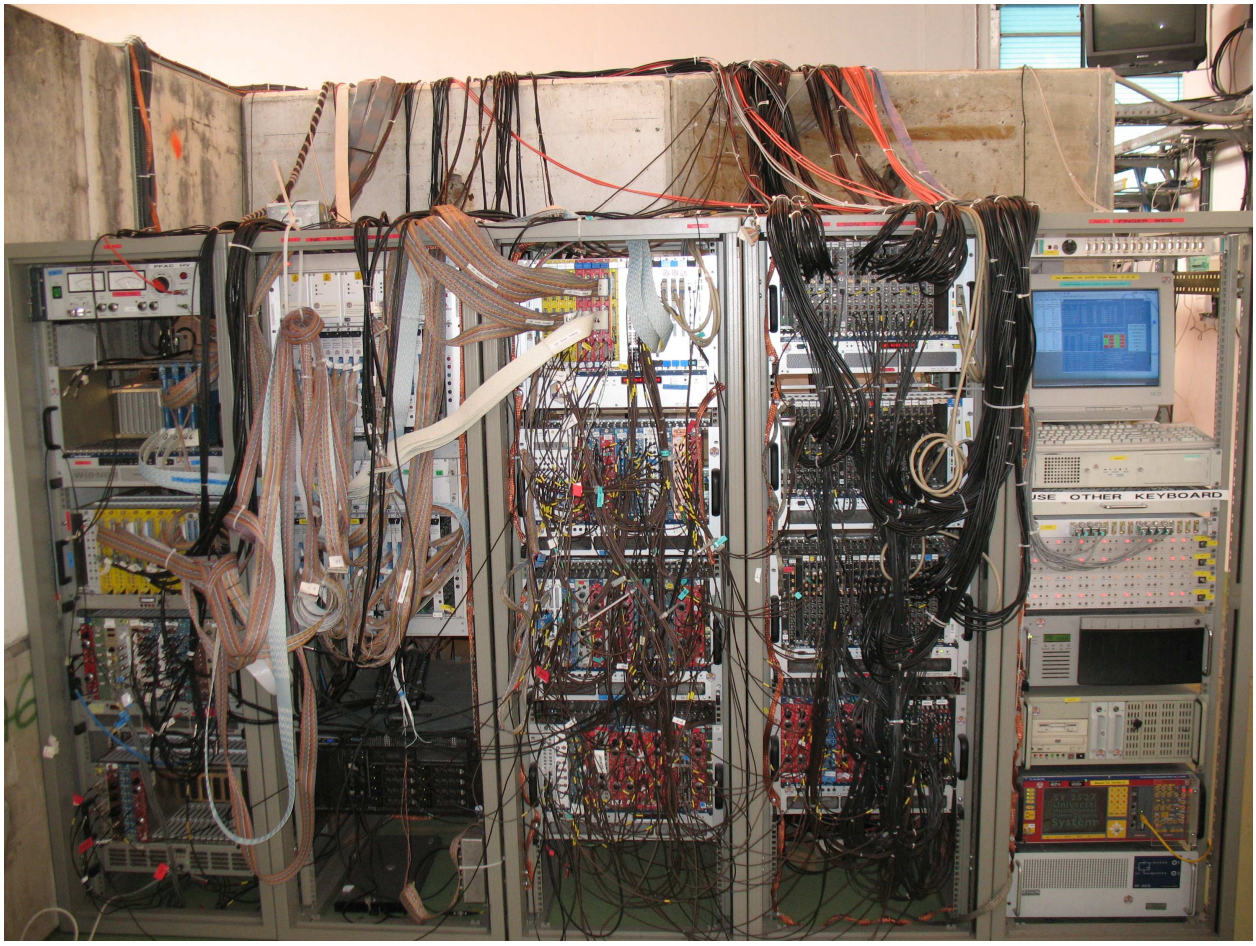

Figure 1: The Miniball electronics in 2010.

The differences to 2004 to 2005 have been indicated, notably the addition of laser on/off bits in the pattern unit and the Munich ionisation chamber, and changes in the TDC cabling. That means it is different to all previous experiments and is likely to be different to future ones. However, there should be certain similarities.

The electronics for this setup has grown gradually rather than being thought out as a single setup, so modules were not necessarily placed in the optimal position in the crates. In places, signals were duplicated due to different people building different parts of the setup and not realizing that the signal they were constructing was already available elsewhere.

In November 2004, a part of the electronics was dismounted and sent to GSI, Darmstadt, and the racks were all moved in order to allow for the building work to extend the ISOLDE hall. However, care was taken then to label things, so that they could be put back together. In May 2005, we put the things back together and it is believed that the state of November 2004 was achieved. In doing so, we noticed some changes with respect to the July 2004 setup. These all seem to be deliberate improvements.

However, the setup works, so there is no reason to change it for this campaign, but it could be improved on in the future.

Caveat: this document was produced during the setup with all the interruptions that that entails, so it probably contains mistakes. Several mistakes have already been found and corrected. There are likely to be others! Also people were still modifying the electronics while I was noting down the configuration. Use it with caution!

The main difference between the 2003 and 2004 setups is that in 2003 all of the CD was treated as one unit, whereas in 2004, each quadrant was dealt with separately. Also, in 2004 we took the ADC busy directly from the ADC module, whereas in 2003 we generated our own signal which was longer than the one generated by the module. Back then, we thought (erroneously) that the ADC was giving a busy signal which was too short and was the reason for mismatches in the number of ADC gates and the number of timestamper DGF events. In fact, the problem turned out to be due to the DGF sometimes missing the last event, so there was no reason to artificially generate the ADC busy.

Part way through 2005, a change was made to the way the TDCs were triggered. Before this change, a signal was generated from the particles and sent via an NIM to ECL converter to one of the last 16 channels of the TDC. After the modification, flat cables were taken from the MALUs giving the hit pattern in the front part of the CD, combined together in pairs (i.e. 8 signals from 16 rings). However, they weren't cabled very logically, so that for the ADCs had the front part of the CD on channels 0 to 15 and the back on 16 to 27 with 27 to 31 unused, but the TDCs had the back of the CD on channels 0 to 11, 12 to 15 unused and the front on 16 to 23. For 2006, we have adopted the same convention for the TDCs as for the ADCs, so the front is first and the back comes after. Consequently, we removed the NIM to ECL converter that was used for this.

In 2005, we also used the Miniball HV main frame to produce the high voltage for the beam dump detector. Prior to that we used a NIM power supply.

Another minor change in 2006: we moved the TDCs one slot to the left and put the ADC for the ionisation chamber to their right, rather than having the ionisation chamber ADC between the ADCs and TDCs for the CD. We also swapped a VME scaler with NIM inputs and the adjacent VME scaler for the PPAC.

In 2007, all the electronics was moved from the platform down to the new hall. However, very little was changed during this move. The main differences are in the electronics to the Bragg chamber. Also, the ΔE detectors, which have not been used in the last few campaigns, but had been cabled in the electronics racks, were not put in the electronics this time.

At the end of 2007, an extra crate was put into rack 1, which was empty at the start of the 2008 campaign. This has the result of renumbering the bottom crate in that rack. Also an ECL $\rightarrow$ NIM converter in that crate was moved from the first slot to the last, as some additional cables were added for the Munich setup, which were too short otherwise.

The last scaler (Bragg chamber) was modified in 2008. In 2007 it was added as an afterthought and it was not documented. It used a linear amplifier on the analogue signal going to the VME sampling ADC and sent this signal directly into the scaler. The additional amplification made it go above the threshold of the scaler, so it counted. However, this is an ugly way of doing things! In 2008, the logical output of the sampling ADC was used. However, as this signal is needed for the logic, it is only accessible after gating with the GFLT and the DAQ not dead signals. This shouldn't matter, as we don't expect particles in the Bragg chamber when there is no beam and we can't count them if the DAQ is dead.

The biggest change in 2008 is to the autofill system. This is especially complicated as it was desired to have both the old and the new systems available. The old system runs on pcepsc22 and the new on the old DAQ computer pcepuis20. The old system uses ISA cards inside the DAQ computer with two flat cables which connect to manifolds B and D (a small flat cable connects A with B and C with D). The new system uses an external USB unit with two flat cables, which are pin-to-pin compatible with the old system and likewise go to manifolds B and D. The old system uses a custom-made PT100 box which is connected to the PC with a flat cable. The new system uses a different PT100 box, which is connected by two USB cables.

In May 2009 the CAEN V785 VME ADCs were replaced with Mesytech MADC32 modules. These modules are capable of timestamping the data with a 40 MHz clock like the DGFs, so it should be possible in future to do away with the timestamper DGFs. However, for the 2009 campaign, we retain both possibilities. i.e. the gate sent to the Mesytech ADCs is sent to the signal input of a DGF to generate a timestamp. This should be approximately the same as the timestamp from the Mesytech's own clock. So this data is duplicated in the list mode. If the Mesytech data proves reliable, we can in future campaigns leave out the timestamper DGFs. Note, however, that the timestamper DGFs for the EBIS, T1 and PS signals have to remain. For convenience and to allow a fast switch back to the CAEN modules if the Mesytech modules don't work, the same VME addresses have been used for both, so it is just a matter of switching the modules and taking the Marabou configuration from 2008.

The differences from 2009 to 2010 are mainly because the T-REX setup was installed in the autumn and I have tried to set up the Coulex setup without dismantling too much of the T-REX setup. As a result, there is an extra crate in rack 4 and the modules are in different places in those crates. Also, we inadvertently shifted all the ADCs and TDCs one slot to the left in the VME crate R3.C1.

2 Notation

I have used the notation "R2.C4.S13" to mean rack two (starting at 1 nearest the wall) crate four (starting with 1 at the top), slot 13. Similarly "R2.C4" means all of crate four of rack two. In the diagrams, the location of the modules is indicated in magenta.

3 The CD cabling

There are two crates of RAL109 shaping amplifier modules. The top one (R2.C1) is for the 16 front rings and the bottom one (R2.C2) is for the 24 back sectors.

The analogue outputs of the RAL109s for the front go directly to channels 0 to 15 of the Mesytech MADC32 VME ADCs in R3.C1.3-6 (i.e. the lower part of the ADCs).

The analogue outputs of the RAL109s for the back also go directly to channels 16-31 of the same ADCs, but since we only use 12 signals (we combine the 24 sectors per quadrant of the back of the CD into 12 signals, by connecting them pairwise - this is done in the hardware) there are some channels spare. By picking off a couple of the wires from these cables, the CD PAD detector (another RAL109 in R2.C1) and the laser power (from the laser control box) are also put into the ADCs.

The ECL outputs of the RAL109s for the front are connected into the four MALU modules (R1.C2.S17,19,21, 23). From there, the ORO signals are connected via a flat cable, where the ends have been split at the MALU end, to an ECL to NIM converter (R1.C4.S23). Also, flat cables connect the outputs of the MALUs to the CAEN V775 32-channel TDCs in R3.C1.7-10 (channels 0 to 15, i.e. the lower part).

For the back sectors, the ECL outputs are connected directly to the same TDCs on channels 16-31 (i.e. the upper part).

Additionally channels 0 and 1 of the laser box are connected to channels 28 and 29 of the quadrant 1 ADC (R3.C1.S3). It looks like the latter one is the laser power.

The signals from the PAD detector come from a different RAL109 in R2.C1 and should each be connected to channel 30 of the ADCs (R3.C1.S3-6). This is done by splitting off two channels from the flat cable and connecting them individually. However, because of the modification to the cable for quadrant 1 in order to add in the laser power (actually, a new cable was made - it is blue and white, while the others are multicoloured), it looks as though quadrant 1 of the PAD detector isn't connected any more.

Probably, we should make a new cable for quadrant 1, with both the PAD and the laser power.

4 The delayed CD quadrant signal

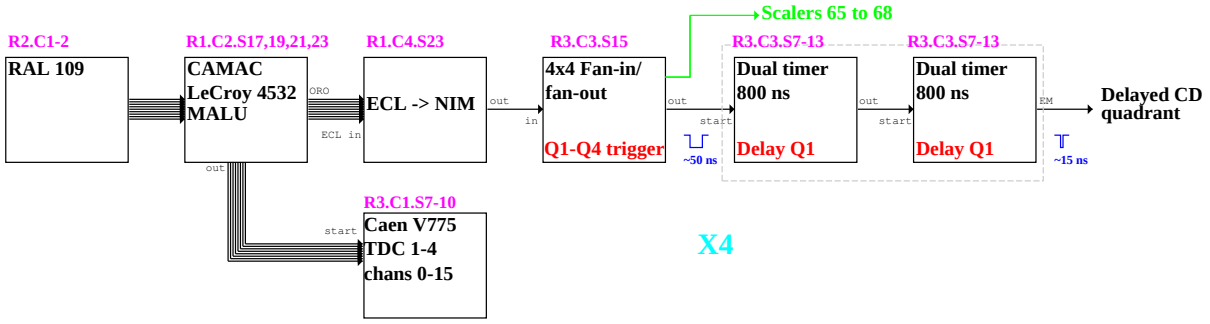

Figure 2: The generation of the delayed CD quadrant signal. This is done for each of the four quadrants of the CD.

From the CD we need to generate logic signals to indicate when an event has occurred in a given quadrant. Note that in previous setups we treated the whole CD as one, but now we treat it as four independent quadrants.

For each quadrant, we take the logic output from the RAL 109 shaper amplifiers via a flat cable to four CAMAC MALU units. Note that although these are CAMAC modules, we do not need to program them, so they are in a crate without a CAMAC crate controller. They just take their power from the CAMAC crate.

Each MALU gives a differential ECL *ORO* output (this is just an OR of all the inputs) and these signals for all four MALUs are combined on a single flat cable and sent to an ECL → NIM converter. From there, the signal for each quadrant goes into one quarter of a 4x4 fan-in/fan-out module and then is used to start a dual timer.

We use two copies of the signal from this fan-out.

- One goes to a scaler. We use scaler 65 for quadrant 1, scaler 66 for quadrant 2 etc.
- One copy is delayed by 800 ns to generate the delayed CD quadrant signal.

We want to delay this signal by 800 ns, but the CAEN dual timers have the property that if a second signal arrives during that time, the end marker comes 800 ns after the **second** signal, not the first. So we use half of a dual timer to generate a signal which is 800 ns wide and then use that to start the second half of the same module also set to 800 ns (so both start more or less simultaneously, but the delaying of the end marker is suppressed). We then take the end marker from the second half of the module. There are probably better ways to do this. In all probability this behaviour of the dual gate is a feature but it doesn't seem to be possible to turn it off and the manual is utterly useless. Perhaps a different kind of gate generator would be better, or a discriminator followed by a gate generator. In future years we should really rethink this part.

For all four quadrants, we use four MALUs, one ECL → NIM converter, one fan-in/fan-out module and four dual timers.

Note that the RAL109s and the NIM crate containing the NIM → ECL converter are in the CD electronics rack, and the CAMAC crate with the MALUs are in the leftmost rack.

Previously, we took a third copy of the signal from the fan-out, passed it through a NIM to ECL converter and used it to start a TDC channel for each quadrant. Some time in 2005 this was changed and now, we take an additional flat cable from each MALU to the corresponding TDC so we have a hit pattern rather than just the OR.

5 Generation of the gamma gate

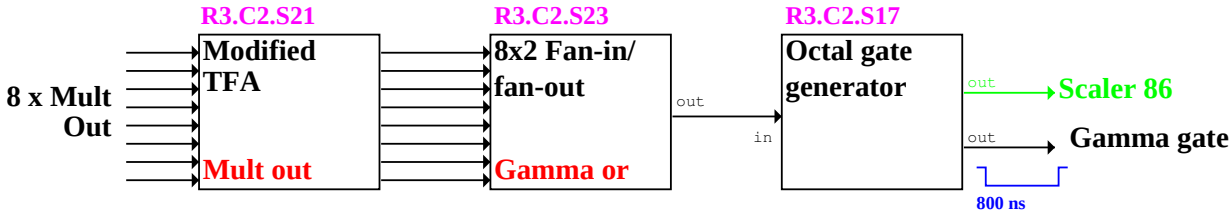

Figure 3: The generation of the gamma gate. This is the logical OR of all the signals from the Ge cores.

We need to generate a signal indicating that one of the Ge detectors has an event. To do this we take the Mult Out (35 mVolt per hit) from the DGF having the first core signal and put it into the Mult In of the next DGF with a core signal (i.e. the third DGF) and from its Mult Out to the DGF with the third core. We then send this signal (i.e. one for each of the eight clusters) to a specially modified TFA (which contains eight Ge preamplifiers set to saturate with a 35 millivolt signal and generate a -0.8 Volt NIM output). In other words, the special module simply converts the 35 mV per hit signal into NIM logic. This signal is passed into a fan-in/fan-out.

This signal is used to generate the particle-gamma coincidence. Note that its width is determined by the DGF parameter *FTPWIDTH*.

6 Generation of triggers

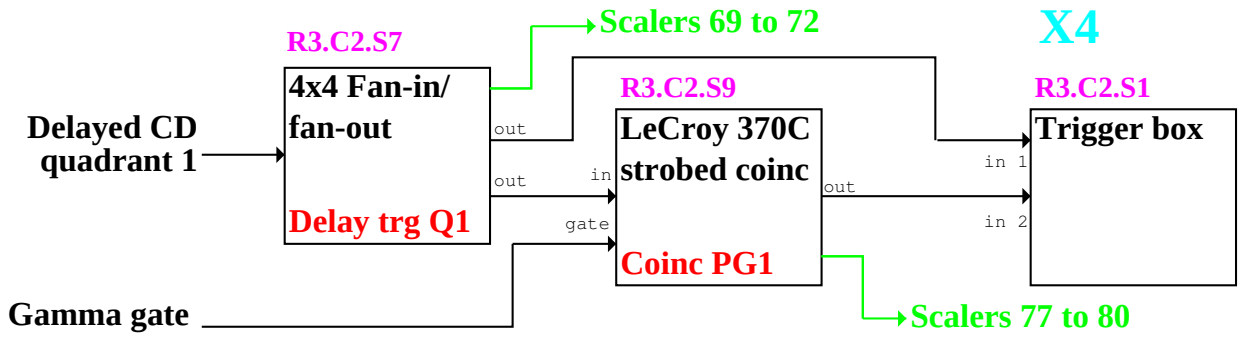

Figure 4: The generation of the triggers. The gamma gate is common to all four quadrants of the CD, but the rest is repeated for each quadrant with the second quadrant using channels 3 and 4 of the trigger box, the third using 5 and 6 and the last quadrant using the two remaining channels 7 and 8.

The delayed CD quadrant signal for each quadrant is passed to a fan-in/fan-out unit (a different quarter of the unit for each quadrant) and for each quadrant, we use three copies of this signal.

- One goes directly to the trigger box where it is downscaled (downscaled particles).
- The second goes into a strobed coinc unit and from there to the trigger box. The strobed coinc unit gates each input (one for each quadrant of the CD) with the gamma gate (see section 5). This gives the particle-γ coincidence.
- The third copy goes to a scaler.

Scaler 69 has the delayed trigger for quadrant 1 and scaler 77 has the particle-γ coincidence for that quadrant. Scalers 70 and 78 have the corresponding signals for the second quadrant etc.

7 Generation of the DAQ dead signals

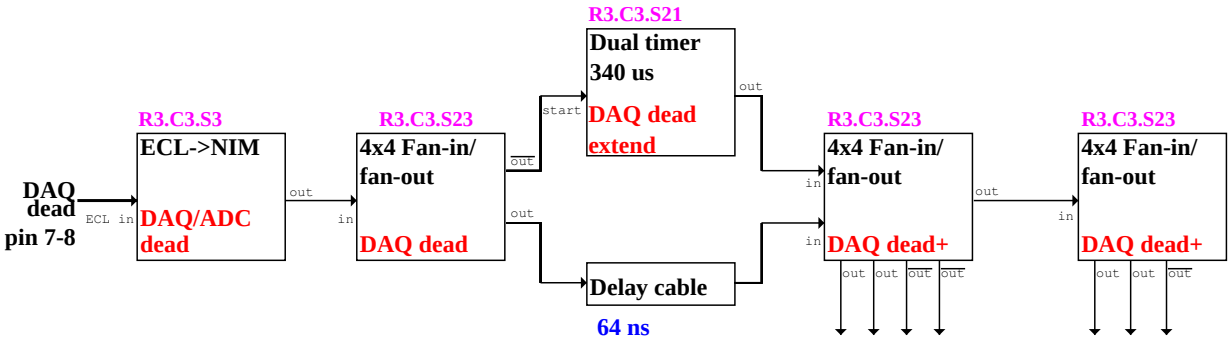

Figure 5: The generation DAQ dead signals.

The VME trigger module has an ECL output indicating that the DAQ is dead on pins 7-8 (note that pins 1-2 are the lower ones and 15-16 the upper ones). This goes through an ECL to NIM converter, after which it is split into two. One part is delayed by a 64 ns cable and the other part is used to start a gate at the end of the DAQ dead time. The idea is to extend the DAQ dead produced by the VME trigger by a fixed amount. If we were to do this without the delay, we might get a short glitch where it goes not dead between the end of the output from the VME trigger module and the beginning of the extension. After that it is fanned out.

In 2007, the DAQ dead extend was 340 μs.

This bit was changed quite a lot between July and November 2004. We use seven DAQ dead signals, three of which are inverted. These come from the top two halves of the fan-in/fan-out in R3.C3.S23. The four normal outputs are used to veto the LeCroy 465 AND modules in R3.C2.S13 and R3.C2.S15 (one for each quadrant of the CD - note that the ANDs are triple modules, so the three quadrants are on one module and the fourth on the other). The three inverted outputs are used to generate the "not busy" signal (R4.C4.S11), the "DAQ trig if DAQ not busy" (R3.C2.S15) and the "Ion and not DAQ dead" (R3.C3.S19).

8 Generation of the DAQ trigger

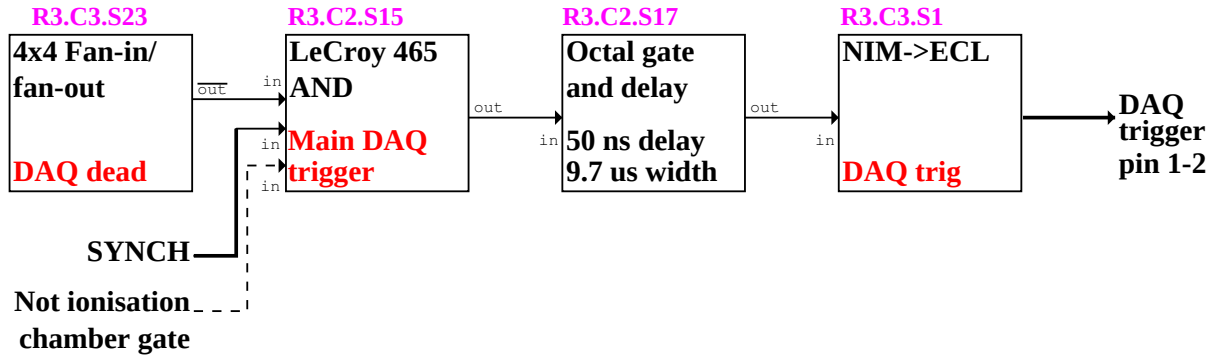

Figure 6: The generation DAQ trigger. The ionisation chamber part is shown dashed because it was not present for all experiments.

We use the DGF SYNCH to trigger readout (having ensured that we force a SYNCH at the end of the on/off window etc. - see section 21) However, if we send a DAQ trigger while the DAQ is busy, the trigger module ignores it, so we need to postpone the DAQ trigger until the DAQ is no longer busy, otherwise it hangs. Since the SYNCH remains set until readout occurs, we AND this signal with the inverted DAQ dead signal, so that the moment we have both SYNCH and the DAQ is live, we generate a DAQ trigger.

The NIM → ECL converter module is the same one used for the ADC busy lines and we have a special flat cable which connects the four ADC busy lines and the DAQ dead output from the VME trigger module to different channels of this unit. We use the first trigger (pins 1-2, which are the lower ones of the ECL input on the VME trigger module).

It seems that between July and November 2004, this bit was changed a little, presumably to prevent deadlocks in the DAQ.

9 Generation of the ADC gates and the TDC stops

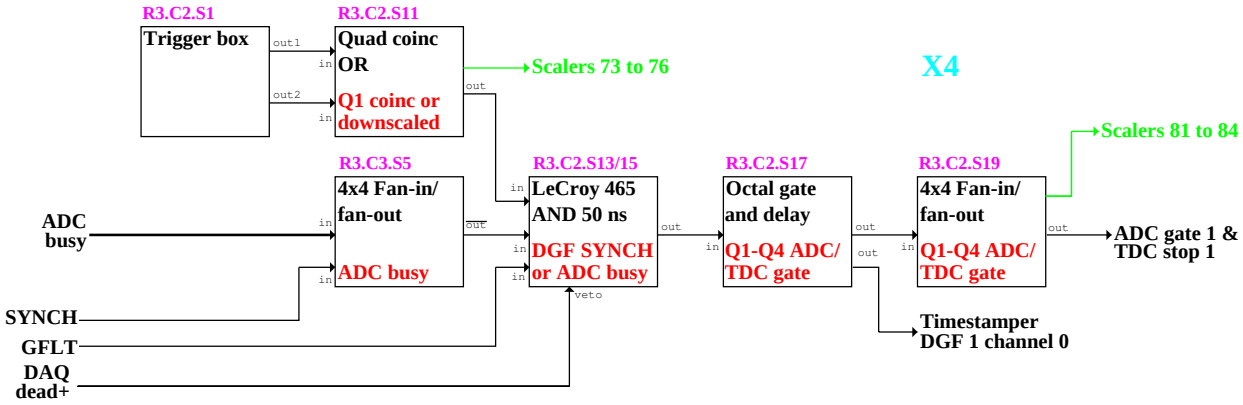

Figure 7: The generation of the ADC gates and TDC stops. Note that we have separate gates for each quadrant of the CD. This diagram shows the connections for the first quadrant. For the second quadrant we use channels 3 and 4 of the trigger box and so on. Note that for the MADC32, the busy signal is NIM, so the ECL to NIM converter is not needed.

In 2003 the ADC gate and TDC stop was the same for all parts of the CD, but in 2004 we changed it to have separate gates for each quadrant.

We want to generate an ADC gate, a TDC stop and a signal for the timestamper DGF corresponding to a given quadrant (four separate gates, four separate stops and four timestamping DGFs) all of the following conditions are satisfied:

- The trigger box gave a signal for that quadrant. Note that we can have both downscaled particle and particle-γ coincidence for the quadrant and these need to be ORed together.
- We are in the on window or the off window. This is the equivalent of the GFLT signal sent to the DGF.
- The ADC for that quadrant is **not** busy.
- The DGF is **not** busy (indicated by the DGF SYNCH signal).
- The DAQ is **not** dead (indicated by the VME trigger module).

The ADC busy signal is provided via a special flat cable which takes the ECL signal from each ADC to a single ECL $\rightarrow$ NIM converter. Note that the DAQ dead signal coming from the VME trigger module is also on the same cable and uses the same ECL $\rightarrow$ NIM converter.

Note also that in 2003 we generated an artificial ADC busy which started at the same time as the real one, but lasted longer. In 2004 we used the real ADC busy signal.

The ADC gate is taken directly from the fan-in/fan-out module at the end of figure 7 and sent to the Mesytech MADC32 gate input. Then another cable goes from the gate output to the TDC corresponding to the same quadrant.

Note that the width of the output of "DGF SYNCH or ADC busy" (R3.C2.S13/15) needs to be set to about 50 ns, not for the sake of the ADC gate and TDC stop, whose signal width is determined by the gate generator, but because these signals are ORed together to make the "Si OR" signal which is used as the pattern unit's control signal. Since there is only a fan-in/fan-out between the "DGF SYNCH or ADC busy" and the pattern control, it is here where we set the width for the signal going into the pattern unit, which needs to be at least 50 ns.

10 Generation of the EBIS window

Note: The "EBIS window" is the window provided by a signal from the EBIS saying there is a bunch of particles incident on the target. The terms "on window" and "off window" refer to two measuring periods of the same length, one on beam the other off beam. Consequently "EBIS window" and "on window" are synonymous terms.

A TTL signal is sent from the EBIS which after conversion to NIM is used to generate an 800 μs gate. The length of this gate needs to be set for the particular experiment to match the opening time of the EBIS gate.

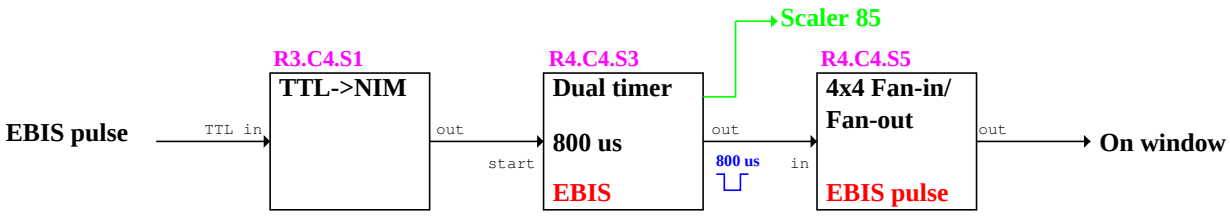

Figure 8: The generation of the EBIS window (on window)

For some reason, in 2006, we found that the dual timer was sometimes triggering on the trailing flank of the EBIS pulse as well as the leading flank, so we put it through a discriminator with a width longer than the width of the signal sent to us from the platform. Note that in this particular case, the pulse coming from the platform was 1.2 ms long, while the EBIS gate was 800 μs long. There was no point in increasing the EBIS gate to 1.2 ms, because there were no particles during that time.

11 Generation of the off window

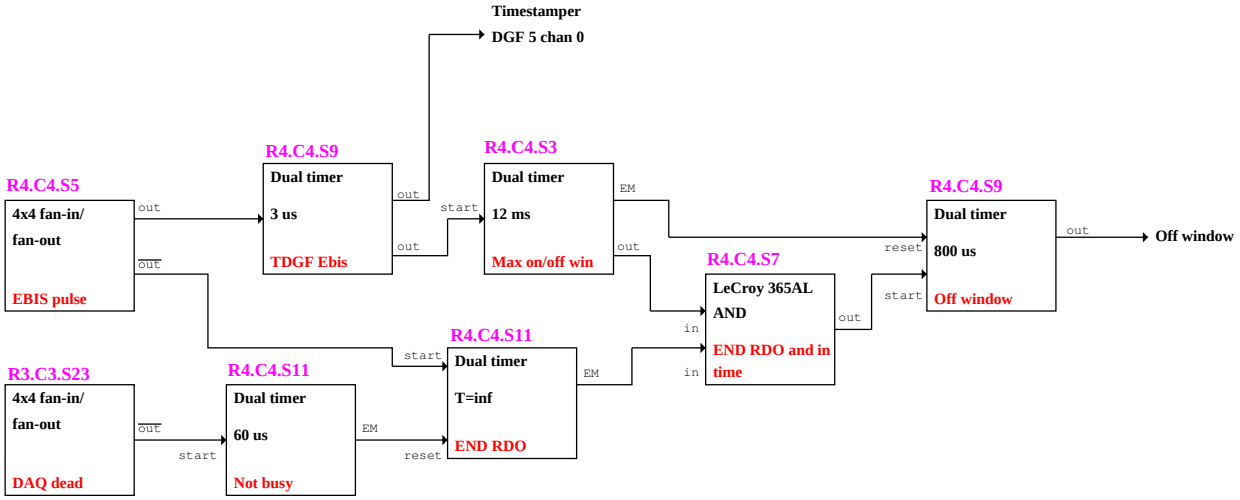

Figure 9: The generation of the off window

We want to open one window when the EBIS gate is open (the on window) then read out the data and then open a second window (the off window) in the gap between EBIS pulses and read that data out in time to be ready for the next EBIS pulse. The on window and off window must be of equal length, so the off window length needs to be set to same as the EBIS gate.

When the EBIS signal comes, we send a 3 μs pulse to the timestamping DGF (note that this was 5 μs in 2003) and start a gate which is closed by the end of readout (the readout being forced at the end of the on window). We also start another gate, called "max on/off window", which is closed before the next EBIS pulse (12 ms in this case, but again this has been 10 ms or 12.25 ms in other experiments). This is used to truncate the off window, so we should also allow some time for reading out the off window data, in order to be ready to acquire when the next EBIS pulse comes. However, normally, it should be possible for the off window to close and readout to complete long before the next EBIS pulse.

Note that the length of the max on/off window should be checked for each experiment. It has to be long enough that there is an on window for each off window, but short enough, to make sure that the off window never gets in the way of the next EBIS pulse (only an issue at high repetition rates).

You can check this easily on the scope by triggering with "EBIS pulse" and looking at "max on/off window" and "GFLT". You should then see one GFLT pulse when the EBIS pulse comes and a second one after it, but before the end of the max on/off window. If max on/off window is too short, this second pulse is suppressed (N.B. the DAQ must be running too, since it is the readout after the off window, which triggers the on window).

In the setup, we use the fact that the end of the on window triggers readout, causing the DAQ to become dead for a while, so we wait until the DAQ is not dead again after the on window.

We start the off window 60 μs after the end of readout (obtained from the disappearance of the DAQ dead signal) to allow the ADCs and TDCs time to start. Note that originally, it was 1 μs but it seems

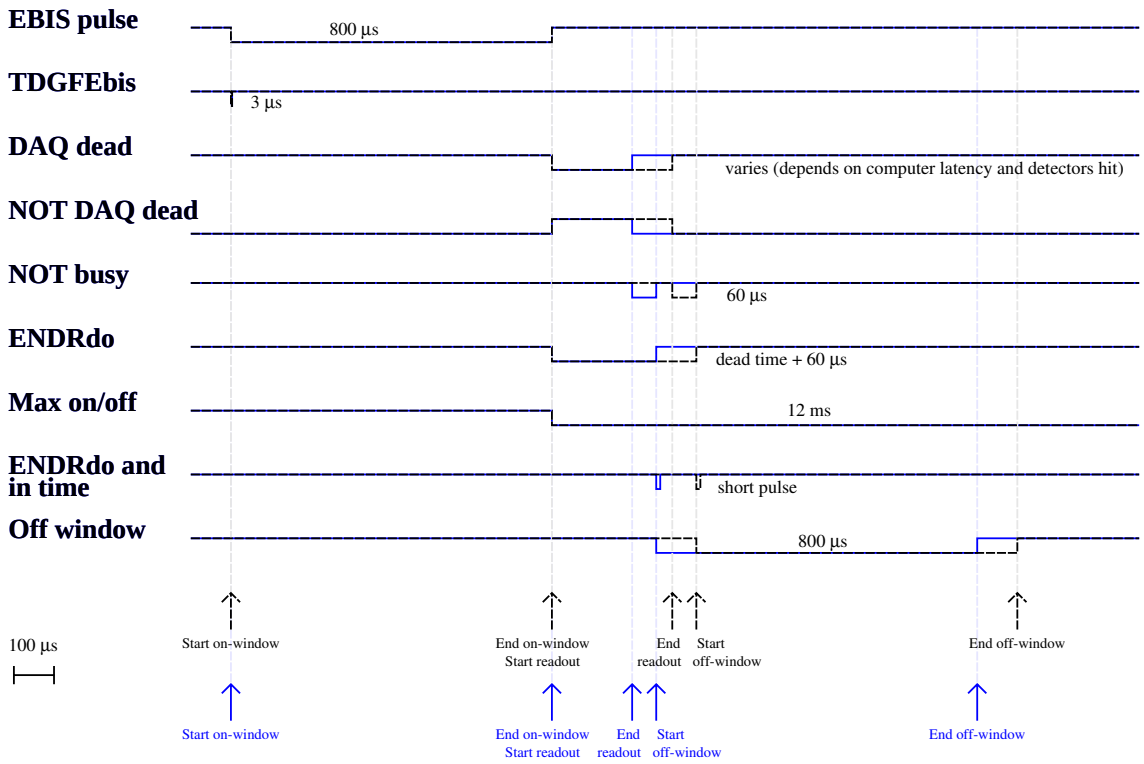

Figure 10: The timing of the off window - the different colours correspond to two different dead times.

that this is not enough time for everything to be ready. Since we have 12 ms in which to open the window, this extra delay isn't a problem. Until we increased this value, the DAQ would hang from time to time. Afterwards it didn't hang nearly as much.

The on window and off window should be of equal length. It is possible to have an on window without an off window, but not the other way round, since the off window is triggered by the first readout within about 12 ms after the on window. Consequently, if there is no on window, the off window also disappears. You should try to avoid this, if possible, by setting the max on/off window appropriately.

To set the two windows to the same width, the easiest thing is to look at the GFLT signal on the scope and if they are not the same length, you will see one width half the time and another the rest of the time, so the trailing edge of the pulse has two vertical lines. When it is correct, you only see a clean NIM pulse. Or you can look at the values of the scalers 1 MHz and on win and 1 MHz and of win, when using the 10 Hz clock as a fake EBIS signal. The former should be 8000 and the latter 16000.

11.1 Multiple off-window mode

In 2008, we did some experiments where the EBIS was triggered by the proton pulse i.e. once every 1.2 seconds at most, but with some of those pulses missing (we had 20 pulses out of 40 in the supercycle, but not equally spaced, so sometimes there was 1.2 seconds between pulses and sometimes as much as 4.8 seconds). We were interested in measuring the radioactive decay after the beam pulse, in order to determine beam composition. However, in the normal configuration of one off window for each on window, this wasn't possible.

So we used a new mode of operation, where the off window is generated not by the EBIS pulse, but by the GFLT signal. This means that an off window is generated not just 60 μs after the end of the readout following an on window (i.e. EBIS pulse) but also following an off window. So then we get an on window followed by a series of off windows up to the limit set by max on/off window. Furthermore, we increased max on/off window from the usual 12 ms to about 1 s (keeping it short enough that it is less than the gap between proton pulses i.e. 1.2 seconds, by enough to allow plenty of time for readout).

To do this, we unplugged the signal coming from the normal output of the EBIS pulse (R4.C4.S5) going to TDGF Ebis (R4.C4.S9) and instead triggered TDGF Ebis from the GFLT output (R4.C4.S13). Then we extended max on/off win (R4.C4.S3) to 1 second.

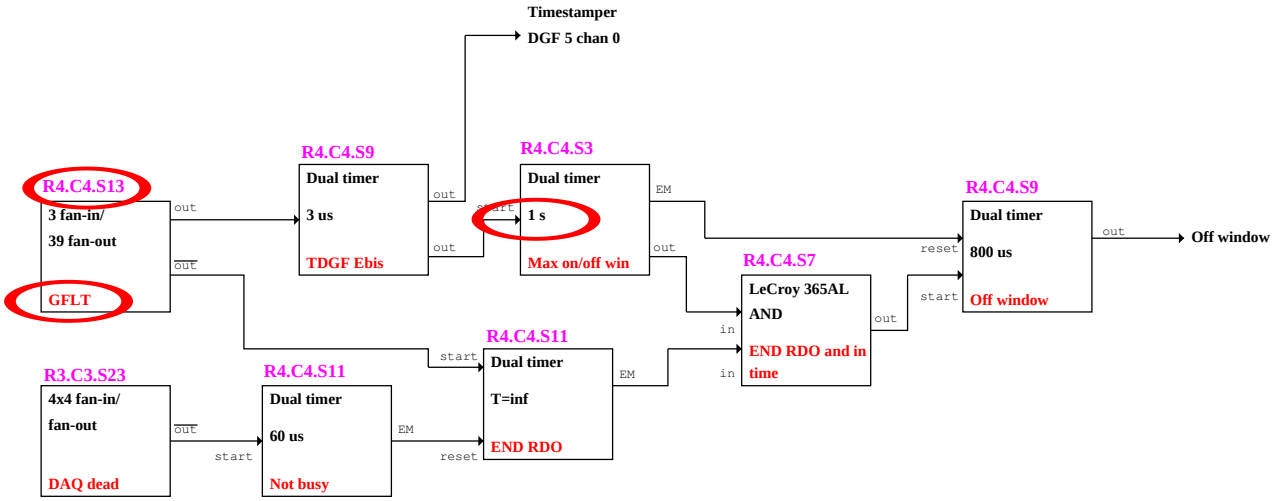

Figure 11: The generation of the multi-off window. The differences compared to the normal off window are highlighted with red elipses

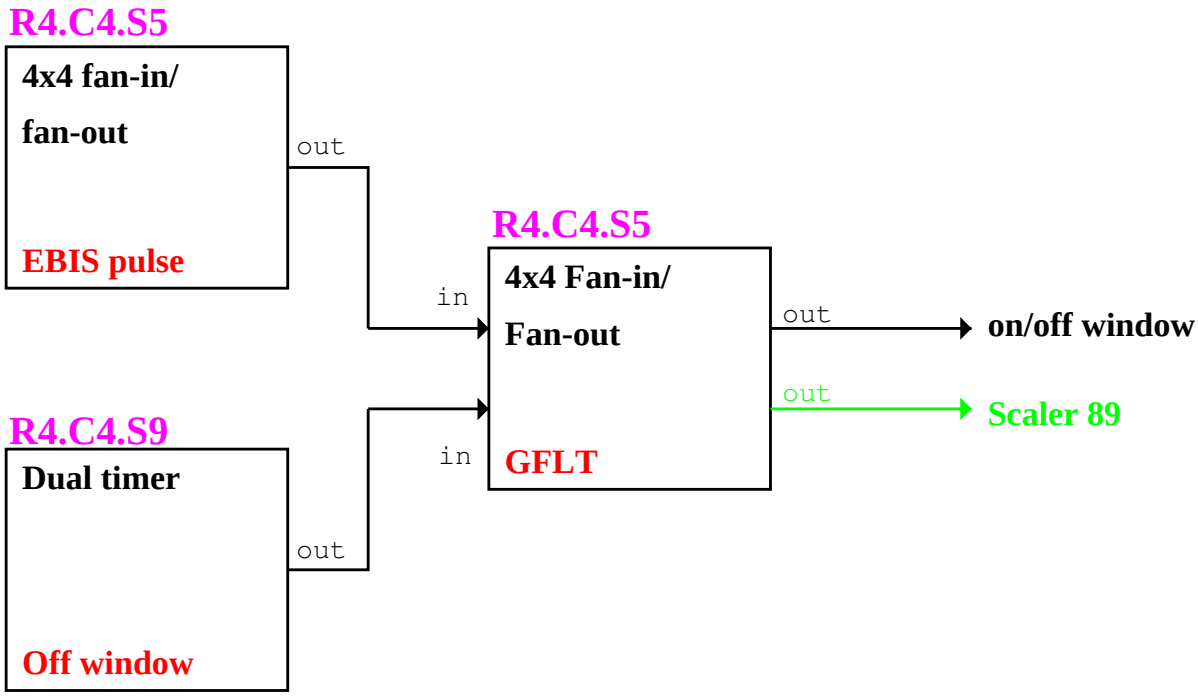

Figure 12: The generation of the on/off window

12 Generation of the on/off window

The on/off window is simply the logical OR of the on window and the off window. It is used to generate the GFLT, so the terms "on/off window" and "GFLT" are synonymous.

13 The generation of the GFLT

The global first level trigger (GFLT) signal which is sent to each DGF is the same thing as the on/off window. We use two 3 fan-in 39 fan-out modules to distribute the signal.

Typical times would be 800 μs on window then about 3.2 ms readout and finally 800 μs off window. The on and off window lengths should be equal and fixed. The readout time varies depending on the events.

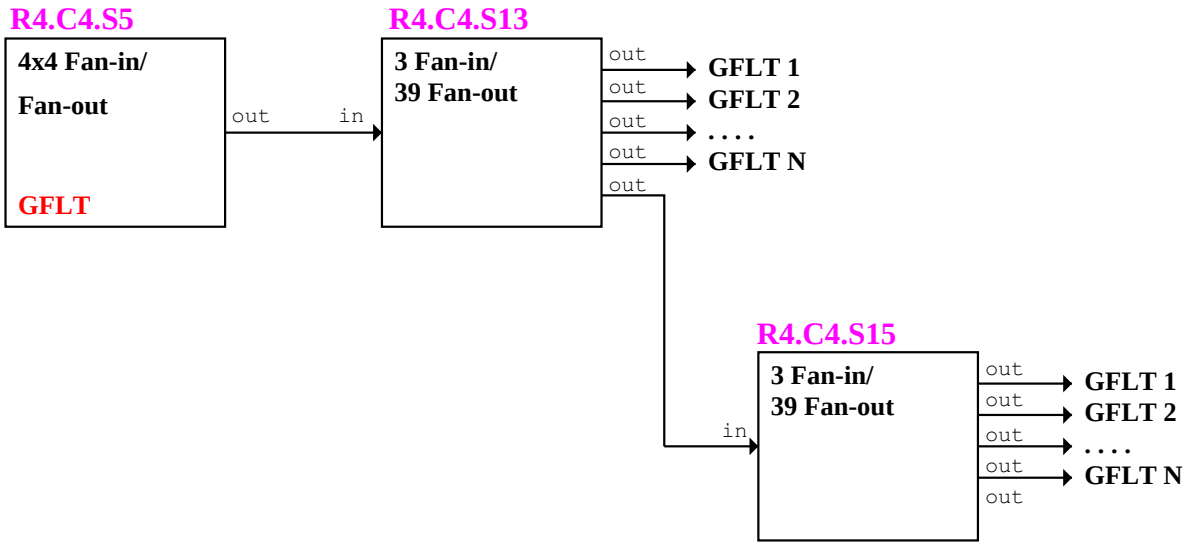

Figure 13: The generation of the GFLT from the on/off window

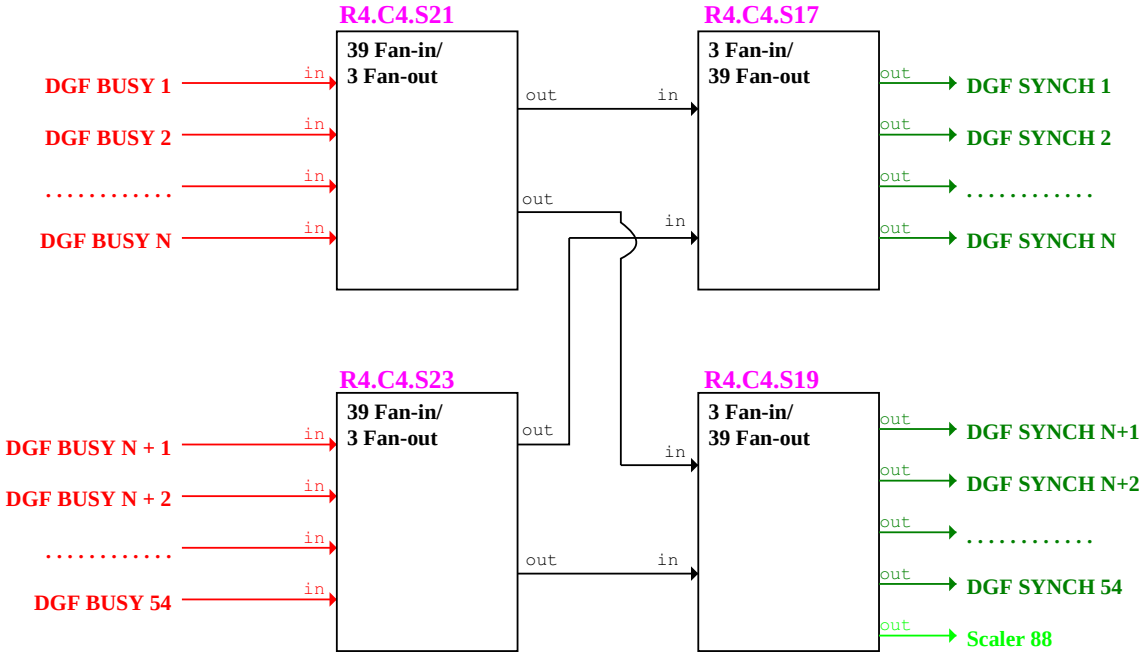

Figure 14: The DGF BUSY/SYNCH loop

14 The DGF BUSY/SYNCH loop

The DGF BUSY/SYNCH loop is made using two 39-fan-in/3-fan-out modules and two 3-fan-in/39-fan-out modules. We take all the BUSY outputs from the DGFs and feed them into the fan-in inputs and then take the outputs to the fan-outs and send the result to each SYNCH input. In this way, if any one DGF is BUSY, the SYNCH line is set to logic one and if all the DGFs are acquiring it is logic zero.

15 Changes for the Mesytech MADC32 modules

Like the DGFs, the Mesytech has an input which can be used to reset the clock. However, they do work in quite the same way, so they cannot be directly integrated into the BUSY-SYNCH loop.

The BUSY/CBUS output of each Mesytech module (R2.C1.S4-7) is connected to the inputs of each of the four parts of the fan-in/fan-out "ADC busy or SYNCH" module in R3.C3.S5. This is the same as for the CAEN modules, as shown on figure 7, except that while the CAEN V785 modules produce an ECL

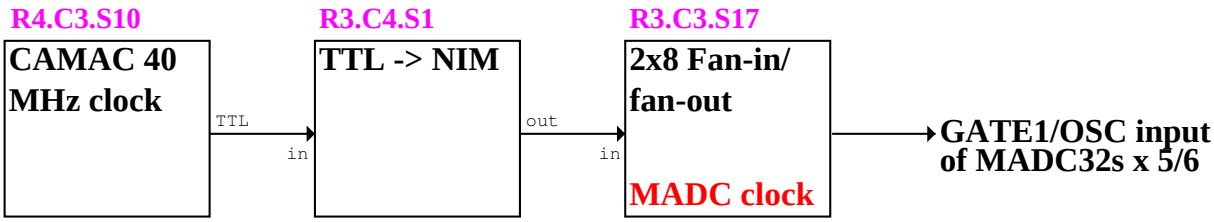

Figure 15: The generation of the 40 MHz clock signal for the MADC. One clock signal goes to each MADC-32. For Coulex there were 5 and for T-REX there were 6.

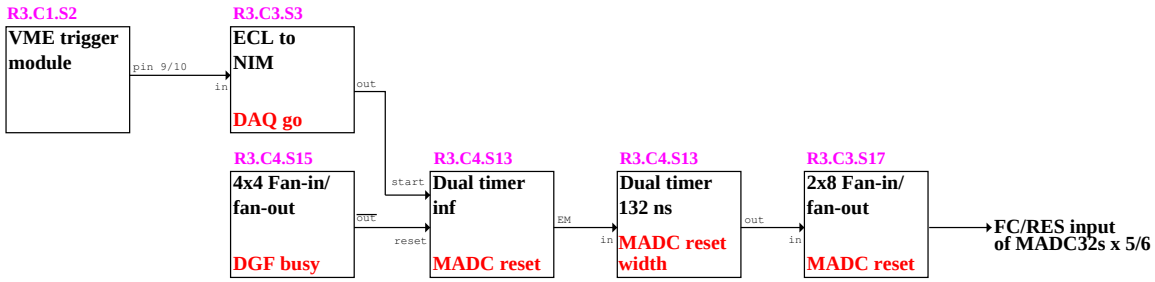

Figure 16: The MADC32 clock reset. One reset signal goes to each MADC-32. For Coulex there were 5 and for T-REX there were 6.

signal, which has to be converted to NIM by the converter in R3.C3.S3, the Mesytech modules generate NIM directly.

The GATE0 input takes the same gate signal as the CAEN V785 from R3.C2.S19, which is also the TDC stop.

The GATE1/OSC input receives the 40 MHz clock, which is taken from a fan-in/fan-out module in R3.C3.S17. This module is in 2x8 mode, because we have five Mesytech MADC32s, which must receive this clock. The input comes from the TTL to NIM converter in R3.C4.S1 and its input comes in turn from the 40 MHz clock module in R4.C3.S10 (i.e. the module which distributes the 40 MHz clocks to the DGFs in that crate). See figure 15.

The FC/RES input is used to reset the clock of the Mesytech module. This signal comes from the second half of the 2x8 fan-in/fan-out module in R3.C3.S17. Again, as we have 5 Mesytech modules, we need five outputs from this module. The input for this module comes from the normal output of the lower part of the dual timer in R3.C4.S13. This part is used just to generate a signal of the appropriate width (set to 130 ns) and is started by the end marker of the upper part of the same module. The upper part is started by the DAQ Go signal and reset by the inverted output of the "DGF busy" signal from R3.C4.S15 with the range set to infinity. i.e. we start the dual timer when the DAQ starts and stop it when the "DGF busy" (which is the logical OR of all the busy outputs of the DGFs) becomes not busy (i.e. the moment when the DGFs reset their clocks) and at that stage it generates the end marker, which is given a long enough width in the lower part of the dual timer and set to the FC/RES input of the MADC32. See figure 16.

The DAQ Go signal is taken from output 6 of the ECL to NIM converter in R3.C3.S3. This module has a flat cable input, which is split into individual twisted pair wires. The first four are for the ADC busy lines

of the CAEN V785 modules, which are not used when the Mesytech modules are used. The fifth one is for DAQ dead which is connected to pins 7 and 8 of the VME trigger module (R3.C1.S2) and the sixth one is the DAQ Go, which is connected to pins 9 and 10 of the same VME trigger module.

The signal cables (flat cables) are connected in the same way as the CAEN V785 modules.

16 Note about special signals

We get several signals from different parts of the REX ISOLDE setup. When ISOLDE is running, we get a T1 signal when a bunch of protons hits the ISOLDE target, then a T2 signal when the gate is opened allowing beam from ISOLDE into REXTRAP. Since these two signals are correlated one-to-one with a fixed time delay between them, it is not necessary to have both. If the laser is running in on/off mode, we get a signal indicating laser on or laser off (sent into the pattern unit).

Note: The T1 and T2 signals are different for each separator (HRS and GPS). You need to hook them up in the ISOLDE control room for the appropriate separator.

The individual bunches of protons hitting the ISOLDE target form part of a supercycle and we receive the PS signal indicating the start of each supercycle. Comparing the T1 pulses to the PS signal indicates how many bunches we receive in each supercycle.

Once the ions have been trapped in the REXTRAP and ionised in the EBIS, the EBIS gate is opened to allow them into the REX accelerator. We receive the EBIS gate signal which indicates when ions are released from the EBIS and which is directly correlated to our beam. Consequently, we use this signal to generate the on-beam window.

17 Generation of the T1 timestamp

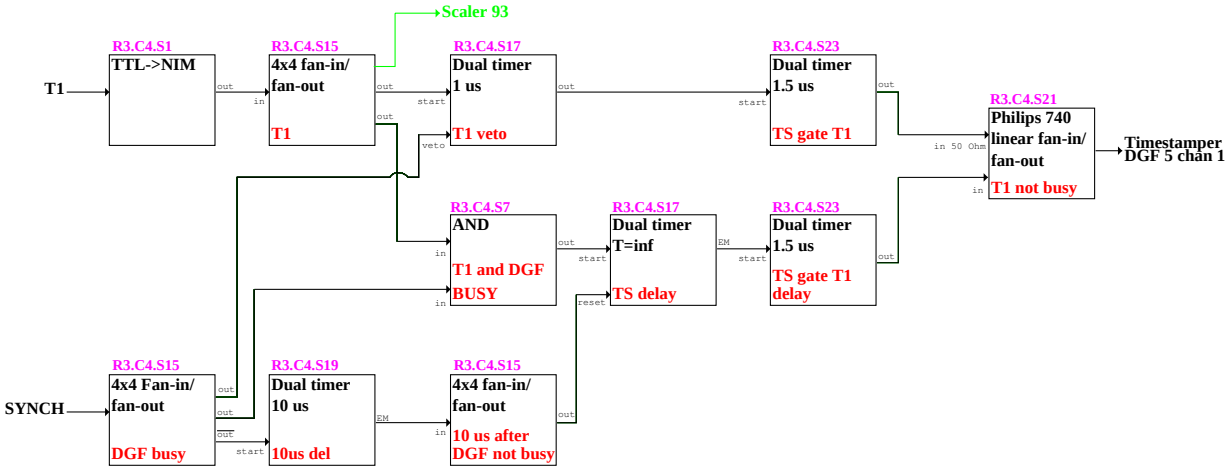

Figure 17: The generation of the T1 timestamp. Note that the three modules at the bottom are the same ones used for the T1 timestamp (see 19).

We want two signals:

- the timestamp of the T1 signal itself , which we obtain by converting it from TTL to NIM and then generating a gate which we send via a linear fan-in/fan-out to the DGF but vetoed by the DGF busy.
- The timestamp of a time 10 μs after the DGF starts acquiring after a T1 pulse.

In order to distinguish the two signals, they are combined using a linear fan-in/fan-out, but with one of them attenuated using a LEMO T-piece with a 50 Ω terminator.

The T1 timestamp is produced in a similar way to the proton supercycle timestamp. Both use the "10 μs after DGF not busy" signal, so the bottom three modules in figures 19 and 17 are the same.

18 Generation of the proton supercycle timestamp

We want to generate a DGF timestamp giving the time of arrival of the proton supercycle start signal and a time 10 μs after the first readout after a proton supercycle start signal.

We receive an TTL signal each time that we get a proton supercycle start which we feed into an TTL $\rightarrow$ NIM converter. We do two things with this signal.

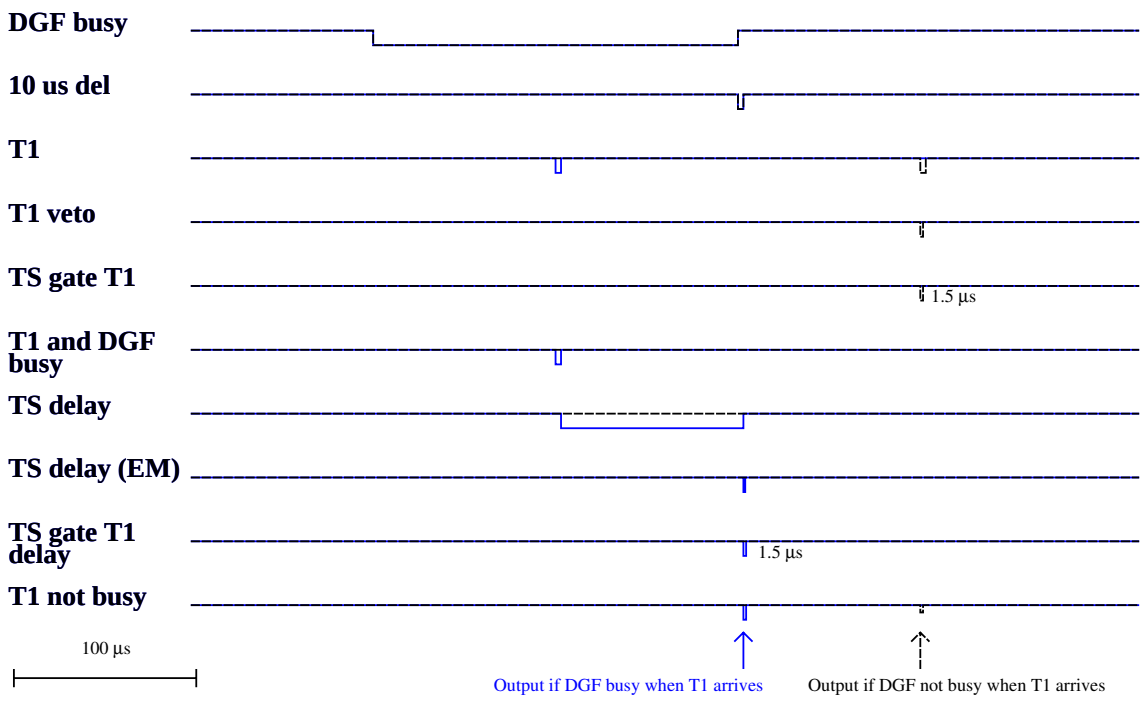

Figure 18: Timings for the T1 timestamp. If the DGF is not busy, when T1 comes, we generate a signal for the DGF at once, otherwise we wait until 10 μs after it becomes not busy. In order to distinguish the two cases, we attenuate the direct one. The different colours show these two cases.

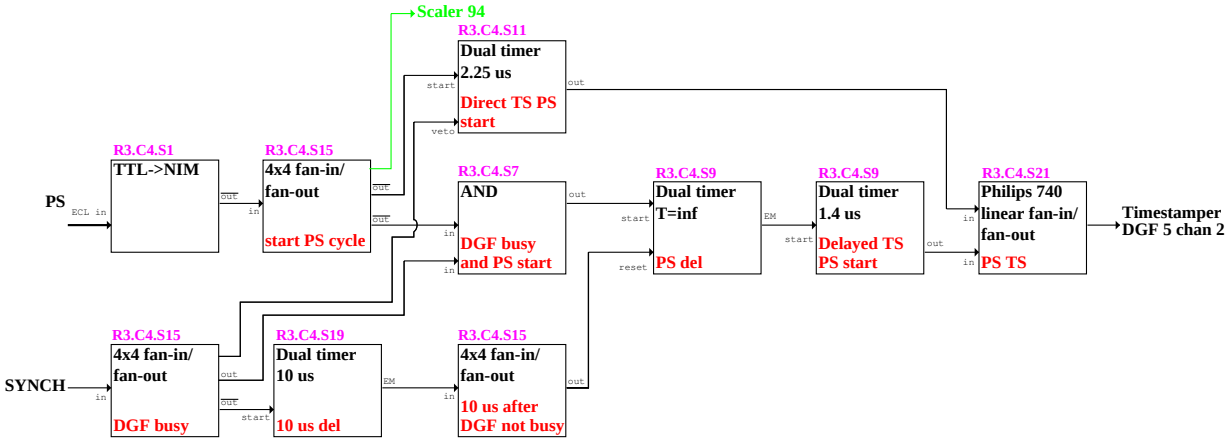

Figure 19: The generation of the proton supercycle timestamp. Note that the three modules at the bottom are the same ones used for the T1 timestamp (see 17).

- Firstly, we use the signal to start a direct gate to indicate the start of the proton supercycle, which we send via a linear fan-in/fan-out to a timestamping DGF.
- Secondly, we want the timestamp for the first time the DGF is not busy after a supercycle start. To get this, we start a timer when the supercycle starts and the DGF is busy, and reset that timer 10 μs after the DGF is no longer busy. Then we use the end marker of that timer to generate a gate, which is sent to the same timestamping DGF via the linear fan-in/fan-out.

Note that the bottom three modules of figures 17 and 19 are the same. i.e. they share the same 10 μs delay.

Why don't we attenuate one of the two inputs to the linear fan-in with a 50 Ω piece in order to get different pulse heights for the two kinds of signal? We do this with the T1 signal and it seems that we should do it to PS as well. I am told this isn't really that important for PS.

I notice that in May 2005, the inverted output from the TTL to NIM converter is being used. This must

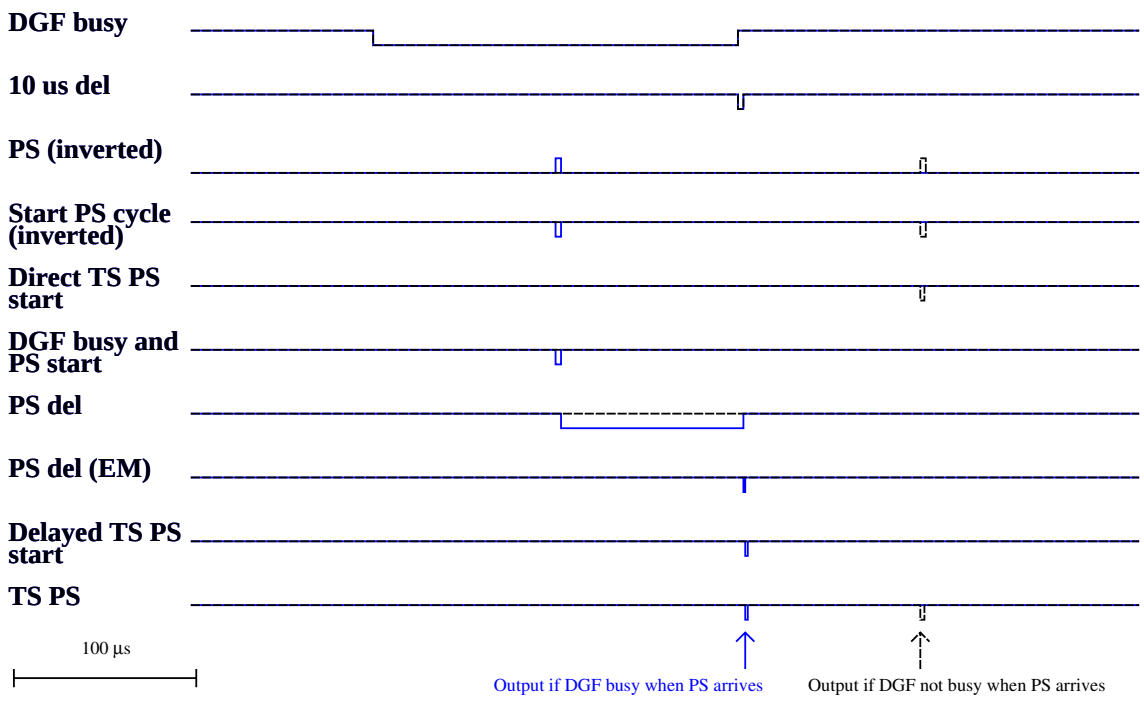

Figure 20: Timings for the proton supercycle timestamp. We generate a pulse for the DGF either when the PS signal comes if the DGF is not busy or 10 μs after it becomes not busy, if it was busy when the PS signal comes. The different colours show these two cases.

have already been like that in November 2004, but I'm not sure if it was like that in July 2004. My notes from July 2004 indicate we used the normal output, but this could be an error. In any case, now we use the inverted output.

19 Generation of the control signals for the scalers

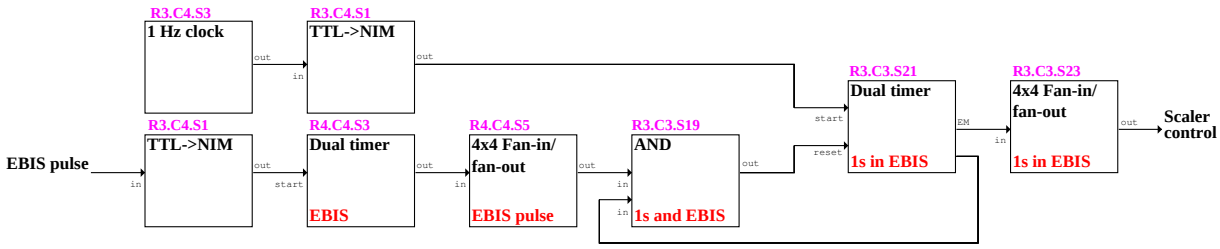

Figure 21: The generation of the control signals for the scalers

Normally, we want to read out the scalers every second. We convert a 1 Hz clock pulse into NIM and use it to start a gate which we fan out to the control inputs for the three scalers.

However, we only want to read when the EBIS pulse comes (on window), so we use the end marker of our gate and reset it with the EBIS pulse.

There was another change here between July and November 2004. An extra AND module was inserted between the fan-in/fan-out module called "EBIS pulse" and the reset for the "1 s in EBIS" dual timer. The other part of the AND comes from the output of that dual timer, so the timer is only reset if it is actually running.

Note, that in 2007, I found that this had been changed from infinity to 316 ms. This is presumably to ensure that the scalers still tick, even if the EBIS is off and as long as the EBIS is running at a higher frequency than about 3 Hz, the dual timer will still be reset by the EBIS pulse before this time is reached. Probably, this was only set to make it possible to debug when the EBIS was off (though normally, we use a fake EBIS pulse for this).

19.1 Scalers in proton-triggered mode

In 2008, we did some experiments where the EBIS was triggered by the proton pulse i.e. once every 1.2 seconds at most, but with some of those pulses missing (we had 20 pulses out of 40 in the supercycle, but not equally spaced, so sometimes there was 1.2 seconds between pulses and sometimes as much as 4.8 seconds). Reading out the scalers every second in such a configuration proved to be rather useless, so we switched to triggering the scalers from the proton pulse T1 rather than the 1 Hz signal. To do this, we unplugged the 1 Hz output from the TTL to NIM converter (R3.C4.S1) and took the signal instead from the "T1" part of the fan-in/fan-out module in R3.C4.S15.

20 Generation of pattern unit control signal

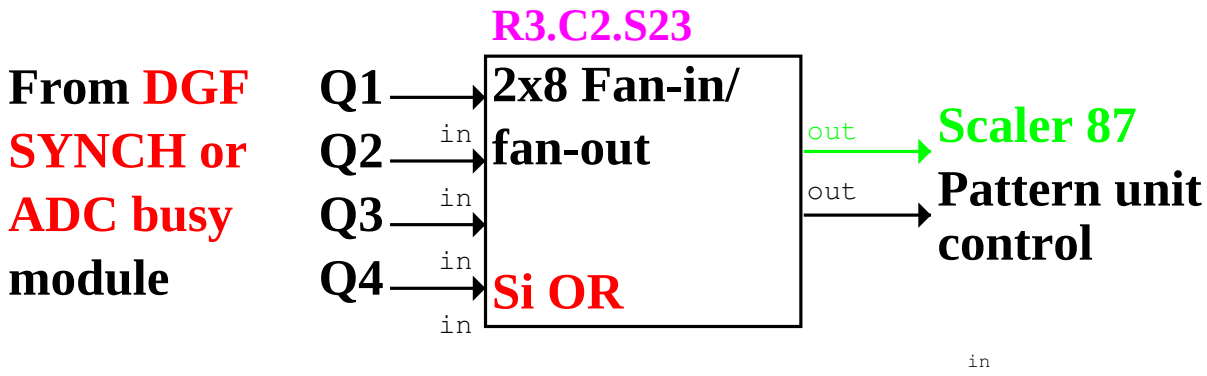

Figure 22: The generation of the control signals for the pattern unit. The four inputs come from the LeCroy 365 AND modules which generate the signal to produce the ADC gate for each quadrant, which is already vetoed by DAQ dead, ADC busy etc.

The pattern unit needs to record the pattern when each ADC gate occurs. However, we only have one pattern unit and four separate ADC gates (one for each quadrant) so we need to OR these signals logically. We take the signal out of the AND "DGF SYNCH or ADC busy" in the middle of figure 7 for each quadrant and pass them into a fan-in/fan-out. The resulting signal is the control for the pattern unit.

Note that the pattern unit needs a signal of at least 50 ns. This width is set in the "DGF SYNCH or ADC busy" modules (R3.C2.S13/15).

21 Generation of the forced readout

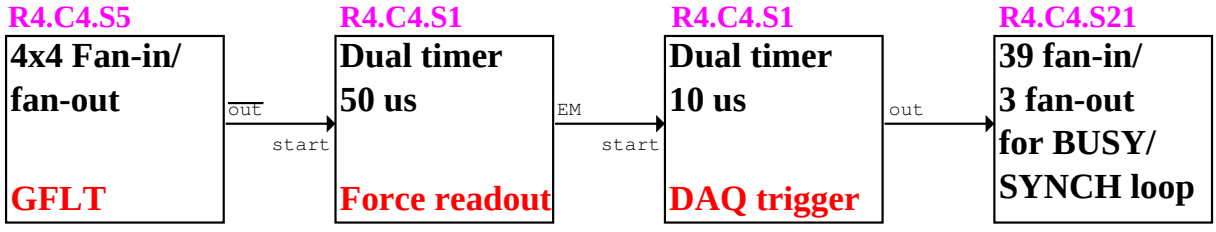

Figure 23: The generation of the forced readout

We take the GFLT signal, delay it 50 μs and then use it to generate a 10 μs wide pulse which we send to the fan-in of the DGF BUSY/SYNCH loop (see section 14). This causes the DGFs to finish their run and since the SYNCH is used to generate the DAQ trigger (see section 8).

Note that in 2004-5, the electronics for this were in rack 3, but they were moved to rack 4 in May 2006 in order to optimise the cables better.

22 The pattern unit bits

The first eight bits of the pattern unit correspond to the eight channels of the trigger box. i.e. downscaled quadrant 1, quadrant 1 and γ, downscaled quadrant 2 ...

In August 2004, we added in the laser on/off signal (bit 9) into the pattern unit. Note that this bit indicates the request that we send to the laser cabin (which is ignored in manual mode) not the actual state of the shutter.

Note that the highest bits should not be used as they are used internally in the acquisition program.

Bit	Signal
1	downscaled quadrant 1
2	quadrant 1 particle γ
3	downscaled quadrant 2
4	quadrant 2 particle γ
5	downscaled quadrant 3
6	quadrant 3 particle γ
7	downscaled quadrant 4
8	quadrant 4 particle γ
9	Laser on

23 Laser on/off

The laser on/off signal is generated from the PS signal, because we want to synchronise with a proton supercycle. The idea is to switch alternately one supercycle laser on, one supercycle with laser off.

In 2003 and 2004, a TTL signal was sent to the laser cabin and used to switch the laser on and off. The box in the laser cabin had a switch "TTL/MAN" which in TTL mode responded to this signal and in MAN mode remained either continuously open or closed according to the state of a second switch (which we left always "open"). The same signal which was sent as TTL to the laser cabin was sent as ECL to the pattern unit. The problem with this is that this means the acquisition records the state that the laser shutter should be in if set to TTL mode. However, if the switch is set to manual, the pattern unit still sees the alternating on/off cycle, even though the shutter is not moving. Furthermore, in 2004 we had the situation where the shutter itself jammed and then the acquisition recorded the state the shutter should have been in, not the actual state.

Another shortcoming of the setup in 2004 was the use of a timer to determine the length of time the shutter should stay open or closed. In fact, the supercycle length varies depending on the number of pulses per supercycle. Also, we don't know if the time between the arrival of the PS signal and the opening of the shutter is short enough if we get the first pulse in the supercycle. It is possible that the laser shutter isn't open fast enough, so that the first pulse is effectively in laser off mode, even though the bit says we are in laser on mode. This is not a problem if somebody else gets the first pulse and we get later ones.

In May 2005 a new system was installed. Now the PS signal is sent directly to some electronics in the laser cabin which does the switching automatically. This electronics is controlled by a control box in R1.C5.S23, to which it is connected by three cables. Depending on the position of the control on this module, the electronics in the laser cabin either sets "laser on", "laser off" or "laser on/off" (i.e. switching at each supercycle) modes. This means we don't have to go to the laser cabin in order to switch between laser on and laser on/off modes.

In addition, there is the laser status signal, which indicates the status of the shutter measured using an optical sensor. In 2005 this was a TTL signal which went through the TTL to NIM converter in R3.C4.S1 and from there up to the pattern unit. In 2006, it was a NIM signal which went directly from the laser cabin, via the control room and the patch panel on the wall into the pattern unit.

In 2007, there was a new shutter, so it was no longer possible to get a feedback of the actual shutter status. Instead, the laser status merely indicates what we have requested. This signal goes through a TTL to NIM converter in R3.C4.S1 and then into the first part of the logic fan-in/fan-out in R3.C4.S5. The inverted output is sent to the pattern unit bit 9 (N.B. the signal from the laser cabin has the opposite polarity compared to 2006, which is why we take the inverted output, so that the bit still is set to mean laser on and cleared to mean laser off as before). An additional copy of this signal (not inverted) is used to veto the 1 MHz (from the same module) using the coincidence module in R3.C3.S19. So this module has only one active input (1 MHz) and the veto (laser not on).

24 1 MHz and EBIS, 1 MHz and GFLT

For some reason these signals weren't documented in 2004. We simply take the logical AND of the 1 MHz clock signal (after conversion from TTL to NIM) and the EBIS signal. Since the EBIS signal is equivalent to the on window, this counts the number of microseconds in the on window. This result is sent to scaler 91. Similarly, we take the AND of the 1 MHz clock and the GFLT, which is equivalent to the on/off window and send it to scaler 92.

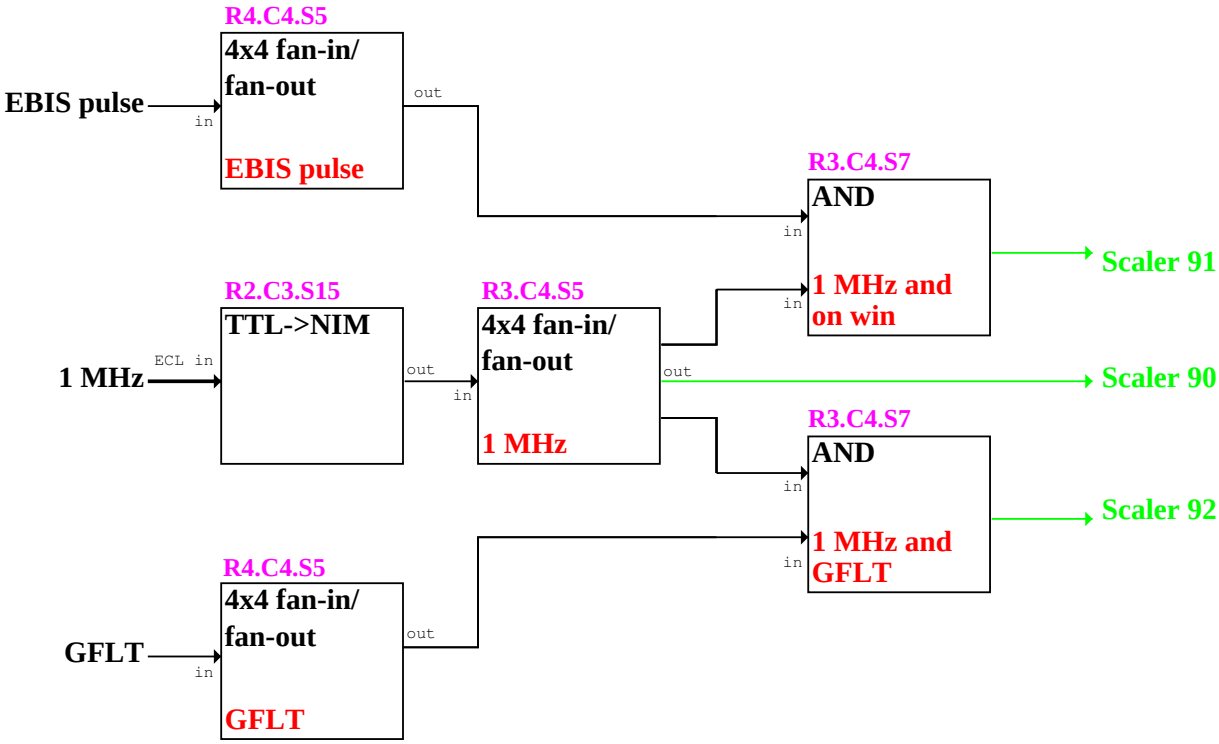

Figure 24: The 1 MHz signals.

This means that we use scaler 90 to measure the time between scaler readouts in microseconds, scaler 91 to give the amount of time the on window was active in that period and scaler 92 gives the sum of the on window and the off window.

25 The DAQ crash reset

In previous years we have frequently observed that the DAQ gets stuck and glitching the button on the coincidence module in R3.C2.S15 would get it going again.

The explanation is probably that this module is used to generate a pulse when the level of the DGF BUSY goes from not busy to busy. This in turn is used to send an interrupt to the power PC to start readout. What we think is happening is that under certain circumstances, the power PC is not ready when the interrupt comes, so it misses it. Then because the levels don't change, no new pulse is generated. Glitching this signal, causes the level to change briefly, creating a new pulse, which triggers the DAQ.

In 2009 we have tried adding a new feature to perform an automatic reset in this case. We take the logical AND of the DGF synch signal (from R4.C4.S17) and the GFLT (R4.C4.S13) using the 4-fold logic unit in R4.C4.S7. The output from this module is fed into the "DAQ dead" fan-in/fan-out in R3.C3.S23. In normal operation, we shouldn't get a GFLT (i.e. an EBIS pulse or an off window) when the DGF is busy and the DAQ is not dead. But we think that when the crash occurs, the DGF is busy and the DAQ is not dead indefinitely, so when the next EBIS pulse comes, this will trigger a DAQ dead and lead to a readout being forced.

This is still under test. If it causes problems, it is enough to unplug the cable labelled "DAQ crash reset" from the "DAQ dead" fan-in/fan-out module in R3.C3.S23.

26 The Bragg chamber

Prior to 2007, the Munich ionisation chamber ran on a different beam line to Miniball and the DAQ was run in a different directory, but the electronics was set up, so it was quick to switch between the two.

In 2007, with the new beam line in the new hall, the system was changed completely. The Bragg chamber now sits permanently at the end of the Miniball beamline and it is intended to acquire it during normal acquisition, so the beam composition can be continuously monitored.

The readout is now performed by a SiS 3300 VME module (R3.C1.S20), which receives the signal from the Bragg chamber directly. In the current version of the DAQ only input 1 is used. The SiS 3330 module provides a trigger from output 1 and needs a gated trigger in input 2. The gating is done in a LRS 465 coincidence unit in NIM R3.C3.S19. Trigger from SIS3300 and DAQ not dead and GFLT.

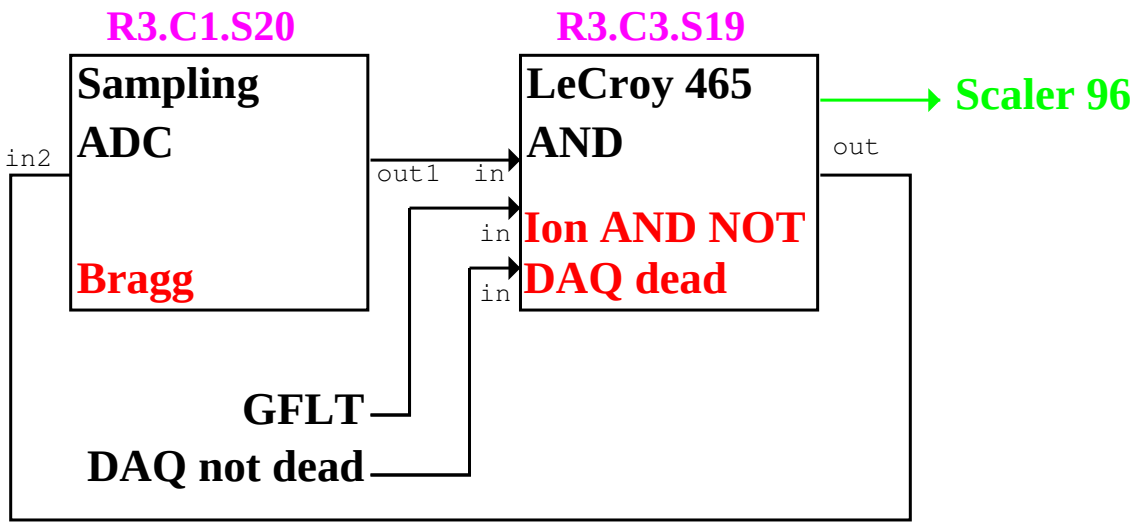

Figure 25: The electronics for the Bragg chamber

27 The ionisation chamber

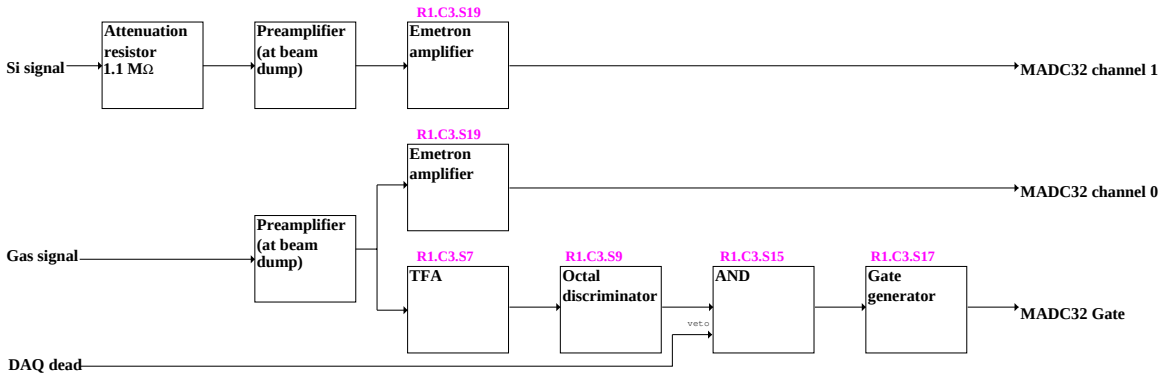

Figure 26: The electronics for the Ionisation chamber

In 2009 we went back to using the ionisation chamber, but this time at the end of the Miniball beam line. There are two signals coming out of the ionisation chamber: the energy loss in the gas (connector at the side of the chamber) and that in the Si detector (at the back). Each of these goes into one of the channels of the preamplifier which sits right on top of the ionisation chamber.

At the electronics rack, the gas signal is split with a LEMO T-piece. One copy goes into a TFA and then one channel of an octal discriminator and from there to a gate generator, which is used to generate the gate for the ADC. The other part goes into one channel of a dual amplifier. The Si signal goes into the other channel of the amplifier and the two signals go to two channels of the ADC.

Previously, we used a CAEN V785 VME ADC, but from 2009 we used the Mesytec MAD32 instead.

28 DGF backplane bus

The DGFs need to have a common 40 MHz clock shared by all modules, which is connected via the backplane bus. This is generated by one of the CAMAC 40 MHz clock modules, which is set to master. Never connect an input to a module set to master. The output of the master goes to the input of another clock set to slave and its output goes to the input of a third module set to slave etc. These connections are made with IEEE-1394 (Firewire) cables at the front.

At the back of these clock modules there are three outputs which can be used to fan out to up to eight DGFs per output. So one module is enough per crate. A flat cable is used to connect each DGF to the clock

with an adaptor piece at one end and a terminator piece at the other.

The DGF has two triggers: a fast trigger sent as soon as an event is detected and a slow DSP trigger sent after the slow filter time (i.e. about 10 μs later. These are available on the same backplane bus as the 40 MHz clock. For Miniball, we have seven signals per capsule on two DGFs, and only the core is allowed to generate a signal. So the trigger lines between those two DGFs need to be connected. Then the core channel can trigger the segments in the same DGF and those in the second DGF. The trigger lines between DGF modules with signals from different clusters should be cut. To do this, physically cut out the four middle wires of the 16 wire flat cable between modules that are not for the same capsule, but leave the other wires (clock etc.) present. Note, that for the special signals for the timestamping DGFs, these are all independent, so all the trigger wires should be cut there.

Unfortunately, because the DGF bus is incorrectly terminated, it was not possible to protect the driver IC of the clock module against misconnection. So if you connect up something wrongly, you will probably blow the AD8017 driver IC for that channel. Don't then swap the channels or you will kill another one!

29 Scalers

There are three 32-channel scaler modules in use. Scalers 1 to 64 are for the PPAC. The third has a variety of different signals from different sources.

Scaler	Signal	Scaler	Signal
65	Q1 free	73	Q1 accepted
66	Q2 free	74	Q2 accepted
67	Q3 free	75	Q3 accepted
68	Q4 free	76	Q4 accepted
69	Q1 delayed	77	Q1 and gamma
70	Q2 delayed	78	Q2 and gamma
71	Q3 delayed	79	Q3 and gamma
72	Q4 delayed	80	Q4 and gamma

Scaler	Signal	Scaler	Signal
81	Q1 gate	89	GFLT
82	Q2 gate	90	1 MHz
83	Q3 gate	91	1 MHz and on win
84	Q4 gate	92	1 MHz and GFLT
85	EBIS pulse	93	T1
86	Total DGF	94	PS
87	Si OR	95	1 MHz and laser on
88	SYNCH	96	Bragg

30 T-REX

There are quite big changes for the T-REX setup, though much of the T-REX electronics can be left during Coulex experiments. An additional crate was added into rack 1 and modules were moved around a bit in that rack. For the most part, there is no reason to move them back when switching to Coulex again, so they can stay that way in the future.

There were also some changes, which were probably caused by people unplugging the existing cables and then plugging in new ones, without noticing that there was already a cable there, that they could have used instead. So hopefully, we can get the two configurations to converge a bit more in future.

The signals are labelled with a "B" for bottom, "T" for top, "L" for left and "R" for right. They are paired off, so that top and left go together and right and bottom go together.

30.1 Trigger generation

The first eight signals "FB ΔE", "FB E", "BB ΔE", "FR ΔE", "FR E", "BR ΔE", "CDE B" and "CDE R" go into the eight channels of an octal discriminator in R1.C4.S11-12. The other eight signals "FT ΔE", "FT E", "BB ΔE", "FL ΔE", "FL E", "BL ΔE", "CDE T" and "CDE L" go into the eight channels of a second octal discriminator in R1.C4.S15-16.

These signals are combined to make two logic signals "BR trigger" and "LT trigger". The four CDE signals are not used. The bottom and right signals are ORed together to make the "BR trigger" using a logic fan-in/out module R1.C4.S13-14 and the top and left signals are ORed in a second logic fan-in/out

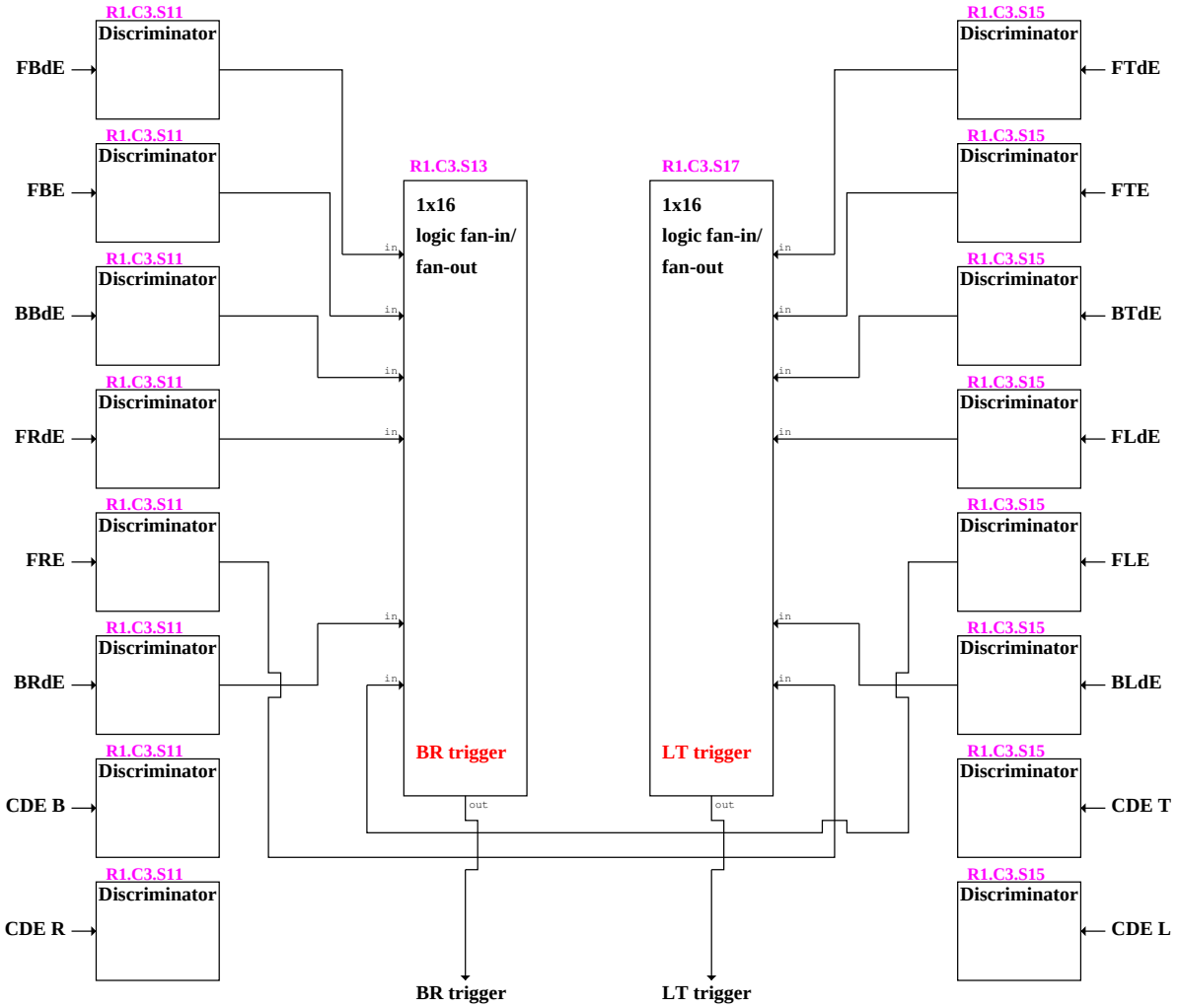

Figure 27: The T-REX trigger signals. Note that the CDE signals go into the discriminator, but the output is not connected anywhere. Note also that FRE and FLE are, for some reason, crossed.

module in R1.C4.S17-18 to make the "LT trigger". Except, that the "FL E" and "FR E" are swapped for some reason, that I do not understand. Perhaps the other end of the cables was swapped?

The particle triggers for Q1 to Q4 come from an ECL to NIM converter in R1.C4.S23 to the four dual timers in R3.C3.S7-14 for Coulex. For T-REX, we unplug the Q1 output from R1.C4.S23 and plug it into the "LT trigger" output of R3.C3.S15-16 and similarly for Q2 as "BR trigger" from R3.C3.S17-18.

In other words, the "LT trigger" in T-REX is equivalent to Q1 in Coulex and "RT trigger" to Q2, with Q3 and Q4 disabled.

30.2 The VME ADCs for T-REX

We use six Mesytec MADC-32 modules as follows:

30.2.1 ADC 1: 0x00F10000

Channel	Meaning
0-15	Strips of top backward E detector (T-E)
15-31	Strips of top forward delta E detector (T-dE)

30.2.2 ADC 2: 0x00F30000

Channel	Meaning
0-15	Strips of left backward E detector (L-E)
15-31	Strips of left forward delta E detector (L-dE)

30.2.3 ADC 3: 0x00F40000

Channel	Meaning
0	not used (wire of flat cable not working???)
1	Rear (i.e. total energy) of top forward delta E detector (T-dE)
2	top forward pad detector (T-P)
3	Rear (i.e. total energy) of top backward E detector (T-E)
4	Rear (i.e. total energy) of left backward E detector (L-E)
5	Rear (i.e. total energy) of left forward delta E detector (L-dE)
6	left forward pad detector (L-P)
7	not used
8	Energy of the first ring with a hit above threshold of the front of top and left quadrant of the CD
9	Ring-ID of the first ring with a hit above threshold of the front of top and left quadrant of the CD
10	Energy of the second ring with a hit above threshold of the front of top and left quadrant of the CD
11	Ring-ID of the second ring with a hit above threshold of the front of top and left quadrant of the CD
12	Energy of the first sector with a hit above threshold of the back of top and left quadrant of the CD
13	Ring-ID of the first sector with a hit above threshold of the back of top and left quadrant of the CD
14	Energy of the second sector with a hit above threshold of the back of top and left quadrant of the CD
15	Ring-ID of the second sector with a hit above threshold of the back of top and left quadrant of the CD

30.2.4 ADC 4: 0x00F50000

Channel	Meaning
0-15	Strips of bottom backward E detector (B-E)
15-31	Strips of bottom forward delta E detector (B-dE)

30.2.5 ADC 5: 0x00F60000

Channel	Meaning
0-15	Strips of right backward E detector (R-E)
15-31	Strips of right forward delta E detector (R-dE)

30.2.6 ADC 6: 0x00F70000

Channel	Meaning
0	Rear (i.e. total energy) of bottom backward E detector (B-E)
1	Rear (i.e. total energy) of bottom forward delta E detector (B-dE)
2	bottom forward pad detector (B-P)
3	not used
4	Rear (i.e. total energy) of right backward E detector (R-E)
5	Rear (i.e. total energy) of right forward delta E detector (R-dE)
6	right forward pad detector (R-P)
7	not used
8	Energy of the first ring with a hit above threshold of the front of bottom and right quadrant of the CD
9	Ring-ID of the first ring with a hit above threshold of the front of bottom and right quadrant of the CD
10	Energy of the second ring with a hit above threshold of the front of bottom and right quadrant of the CD
11	Ring-ID of the second ring with a hit above threshold of the front of bottom and right quadrant of the CD
12	Energy of the first sector with a hit above threshold of the back of bottom and right quadrant of the CD
13	Ring-ID of the first sector with a hit above threshold of the back of bottom and right quadrant of the CD
14	Energy of the second sector with a hit above threshold of the back of bottom and right quadrant of the CD
15	Ring-ID of the second sector with a hit above threshold of the back of bottom and right quadrant of the CD

So the first one is for top, the second for left and the third for top-left and these have the same gate "LT gate" (see below). The fouth is bottom, the fith is right and the sixth is bottom-right, and these three have the "RT gate".

30.3 ADC busy

The logic fan in/out module in R3.C3.S5-6, which runs in 4x4 mode for Coulex, is switched to 2x8 mode. The top half is used to generate the "LT busy" and the bottom half for the "BR busy". We take the busy signals from the first three ADCs (top, left and top-left) in the top half and OR them with the DGF SYNCH signal and another signal from the DAQ, which seems to be a DAQ busy to make the "LT busy". We take the busy signals from the other three ADCs (bottom, right and bottom-right) together with the SYNCH and the DAQ busy to make the "RT busy". The signals which correspond to Q3 and Q4 were unplugged.

In the Coulex setup, this module runs in 4x4 mode with the busy from the ADC for each quadrant being ORed with the SYNCH. We don't OR in any DAQ busy at this stage, because the output of this module goes into the "DGF SYNCH or ADC busy" in R3.C2.S13/15 which is vetoed by the "DAQ dead+" signal. Perhaps it was not realised that this was the case, when the T-REX setup was made and an additional DAQ busy was ORed in unnecessarily?

If it is true that the DAQ busy is not really needed here, it would be possible to switch back to 4x4 mode and OR together the busy signals from the first three ADCs with the SYNCH in the first quarter and the others in the second quarter, leaving the Q3 and Q4 as they were.

30.4 ADC gates

We take the "Q1 ADC/TDC gate" (which is really "LT gate" for T-REX) from R3.C2.S17-18 and pass it to the top half of the logic fan-in/out module in R3.C2.S19-20, as for the Coulex case, but this logic fan is set to 2x8 mode for T-REX rather than the 4x4 mode for Coulex. There seems to be no reason for this, however. There are outputs taken from this fan, one for the gate of each of the first three ADCs and one for scaler 81 and a single quarter of this module in 4x4 mode would be enough to generate these signals. There is, in fact, a fifth cable connected to an output but it is just dangling with nothing on the other end! In any case, the scaler could use the inverted output if really needed.

Similarly, the bottom half of this logic fan-in/out module is used for "Q2 ADC/TDC gate" which is actually "RT gate" and it is used to gate the other three ADCs and to provide the signal for scaler 82.

The signals for Q3 and Q4 as well as scalers 83 and 84 were unplugged.

These changes do not seem necessary. There are enough outputs to use the 4x4 mode and leave Q3 and Q4 connected as in Coulex runs (there will be no signal there anyway).

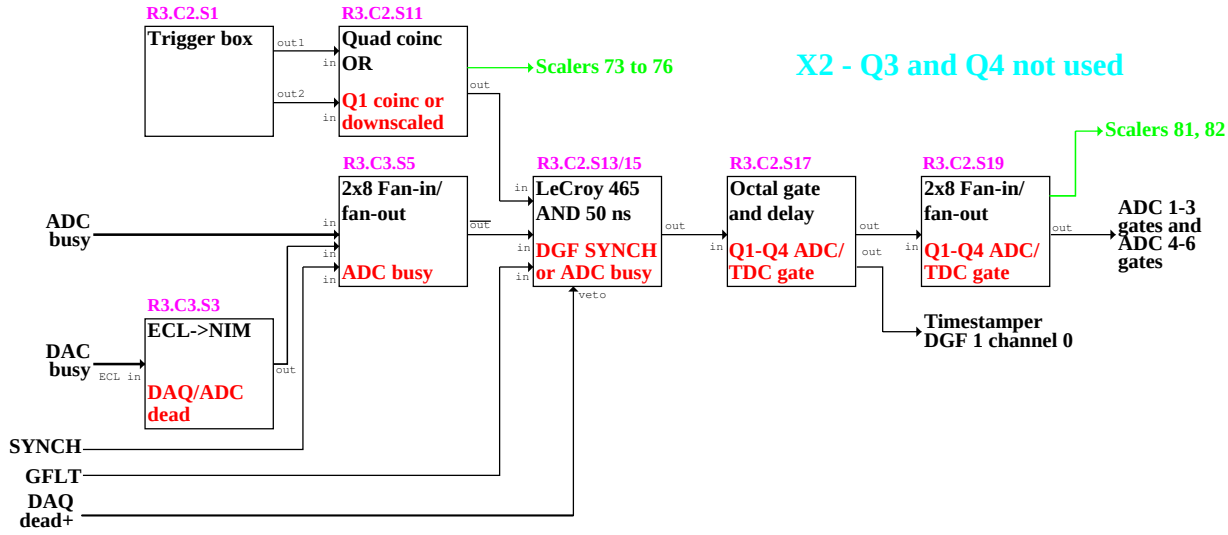

Figure 28: The generation of the ADC gates for the T-REX setup. Note the two fan-in/fan-out modules are in 2x8 mode here, but are in 4x4 mode for Coulex, so the cables are moved around. The upper half is for the LT gate and the lower half for the BR gate, which are equivalent to Q1 and Q2. The Q3 and Q4 signals are not used, so they are partially unplugged. Also there is an additional DAQ busy going into the first fan, which might be superfluous, given that the DGF SYNCH or ADC busy is vetoed by the DAQ dead+ signal. This figure should be compared to figure 7 which is the equivalent for Coulex.

30.5 Diamond active collimator

The diamond detector has 9 pixels and in addition there are four photodiodes.

There is a multiwire cable coming from the diamond detector to a CAEN peak sensing VME ADC in R3.C1.S10 which has the signals from the diamond detector and the photodiodes. This is gated by the EBIS pulse taken from R3.C4.S5-6.

There is also a TTL signal sent to the diamond detector which is started by the GFLT using a dual timer in R3.C4.S19-20 and then converted from NIM to TTL using the converter in R3.C4.S1-2 and then two identical copies of this signal are sent to the target chamber, which are produced in an analog fan-out module in R1.C3.S3-4.

30.5.1 ADC 7: 0x00F80000

Channel	Meaning
0	Top pixel of the diamond
1	Top Left pixel of the diamond
2	Left pixel of the diamond
3	Bottom Left pixel of the diamond
4	Bottom pixel of the diamond
5	Bottom Right pixel of the diamond
6	Right pixel of the diamond
7	Top Right pixel of the diamond
8	Central pixel of the diamond
9	Top Pin-Diode in front of collimator
10	Left Pin-Diode in front of collimator
11	Bottom Pin-Diode in front of collimator
12	Right Pin-Diode in front of collimator

30.6 MADC signals

An additional fast clear is needed for the extra MADC-32. This comes from the 2x8 fan-in/out module in R3.C3.S17-18 just as for the other five.

An additional clock signal is needed for the extra MADC-32. This comes from the 2x8 fan-in/out module in R3.C3.S17-18 just as for the other five.

This module was already in 2x8 mode before, because it had to produce five signals, for the fast clear and five for the clock. So adding a sixth one is trivial.

30.7 Summary of changes

- Extra crate in rack 1
- Trigger logic added (two octal discriminators, two logic fan in/out modules) R1.C4.S11-18.
- Eight STM-16 shapers added (R1.C3.S5-20).
- Six MADC-32s rather than five
- Extra fast clear from R3.C3.S17-18 to the new MADC.
- Extra clock signal from R3.C3.S17-18 to the new MADC.
- Additional CAEN ADC for diamond detector
- TDCs removed
- Busy generation changed. R3.C3.S5-6 switched from 4x4 to 2x8 mode.
- Gate generation changed. R3.C2.S19-20 switched from 4x4 to 2x8 mode.

31 Positions of modules in crates and racks

The racks are numbered from 1 to 5 with 1 being closest to the wall. The crates are numbered from 1 with crate 1 being highest. The notation R1.C2 means rack one crate two and R1.C2.S17 refers to the module in slot 17 of that crate. These numbers are shown on the circuit diagrams.

31.1 Rack 1

Figure 29: R1.C1: PPAC power supply. We normally use about +400 Volts

In rack 1 we have the PPAC HV supply, one camac crate without a crate controller and one NIM crate. Note that this NIM crate is the one which was in R2.C3 in previous years. It was moved to make space for the new DAQ computer.

31.1.1 CAMAC crate R1.C2

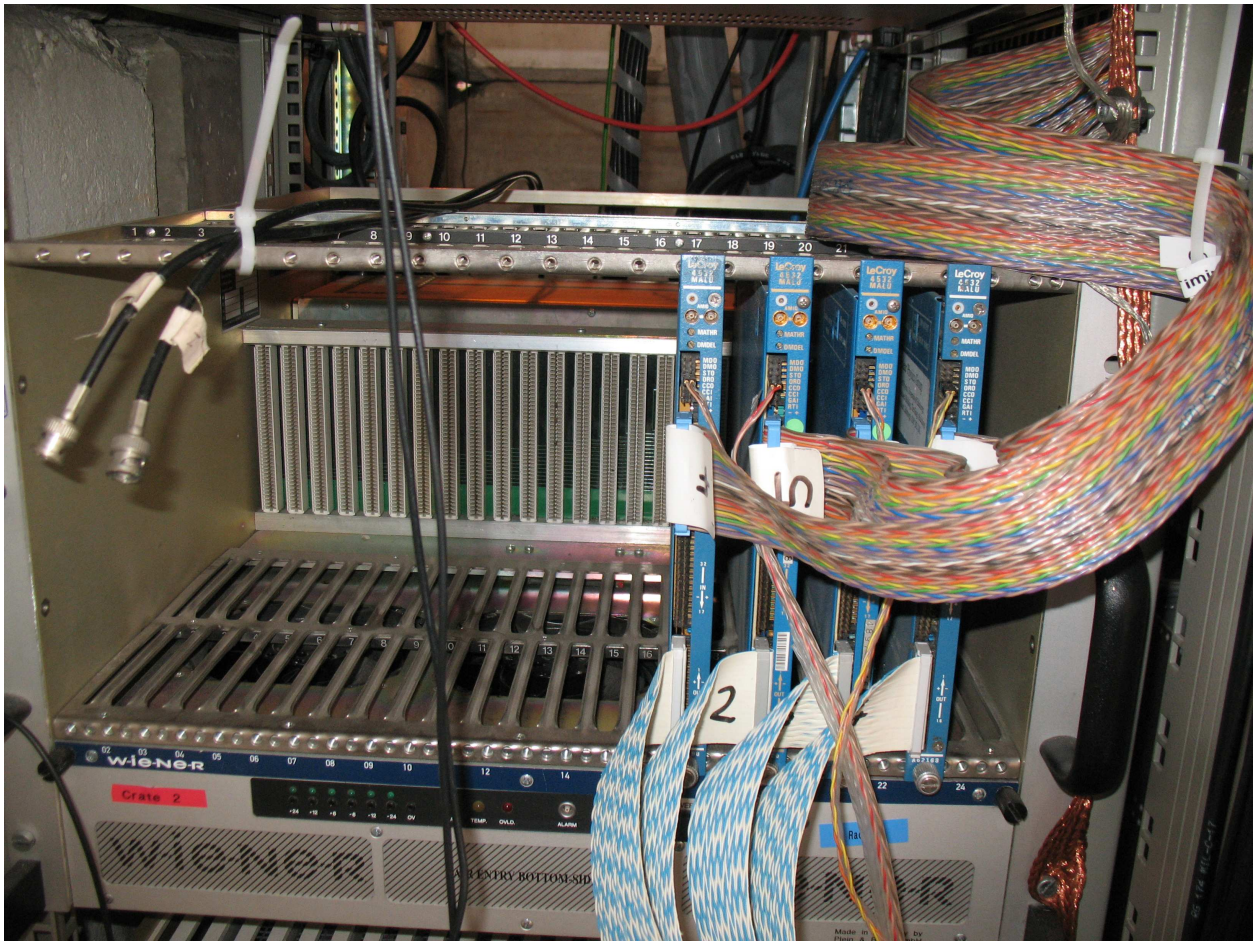

Figure 30: R1.C2: The cabling of MALUs - four multicoloured flat cables (one from each quadrant - the other ends are split in pairs, so they go to 8 RAL109s) come from the RAL109s in R2.C2 (i.e. the front rings) to the inputs. Four blue and white flat cables go from the outputs of the MALU to the TDCs. The ORO output of each MALU goes to the ECL→NIM converter (R1.C4.S23).

- Slot 17 - LeCroy 4532 MALU (Quadrant 1 OR)
- Slot 19 - LeCroy 4532 MALU (Quadrant 2 OR)
- Slot 21 - LeCroy 4532 MALU (Quadrant 3 OR)
- Slot 23 - LeCroy 4532 MALU (Quadrant 4 OR)

31.1.2 NIM crate R1.C3

This crate was used for testing purposes and has nothing which was in use for the first experiment, as this was without laser operation and the laser control was not set up.

- Slot 1-2 empty
- Slot 3-4 TUM analog fan-in/out
- Slot 5-6 Mesytec STM-16 (TΔE)
- Slot 7-8 Mesytec STM-16 (TE)
- Slot 9-10 Mesytec STM-16 (LΔE)
- Slot 11-12 Mesytec STM-16 (LE)
- Slot 13-14 Mesytec STM-16 (BΔE)
- Slot 15-16 Mesytec STM-16 (BE)

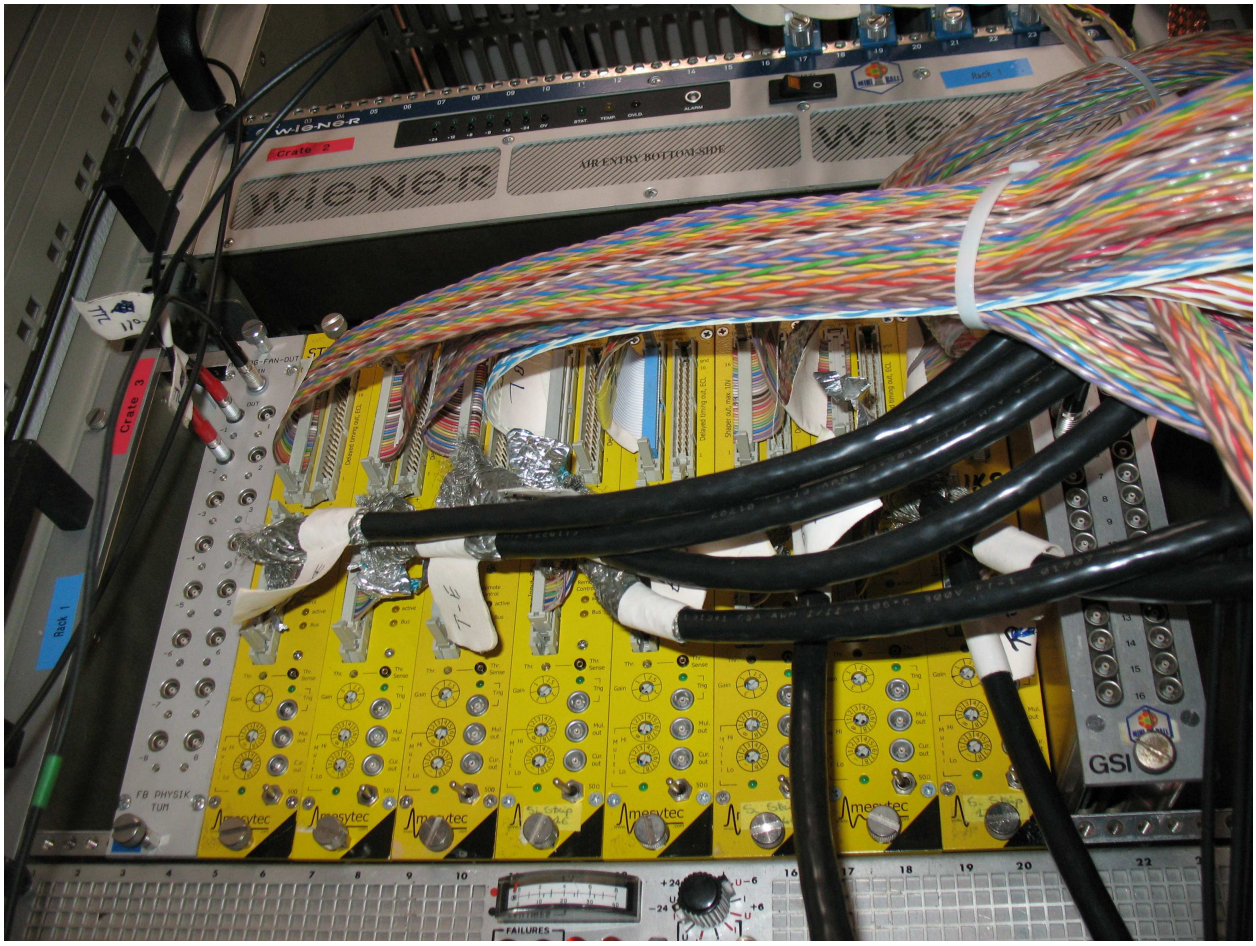

Figure 31: R1.C3: NIM crate - nothing here is used. At this time, the laser control unit was in this crate, but not in use.

- Slot 17-18 Mesytec STM-16 (RΔE)
- Slot 19-20 Mesytec STM-16 (RE)
- Slot 21-22 GSI ECL to NIM converter (not inserted)
- Slot 23-24 empty

31.1.3 NIM crate R1.C4

- Slot 1-2 empty
- Slot 3-4 Sixfold preamp power supply for beam dump detector
- Slot 5-6 Silena quad bias supply (CD bias)
- Slot 7-8 ±24 Volt power
- Slot 9-10 Silena quad bias supply (CD E detector bias)
- Slot 11-12 Philips 705 octal discriminator (BR trigger)
- Slot 13-14 LeCroy 429A logic fan-in/fan-out (BR trigger)
- Slot 15-16 Philips 705 octal discriminator (LT trigger)
- Slot 17-18 LeCroy 429 logic fan-in/fan-out (LT trigger)
- Slot 19-20 Ortec 480 pulser (CD pulser)
- Slot 21-22 Dummy module, with a cable taking power of crate
- Slot 23-24 EC1600 ECL → NIM converter (particle trigger)

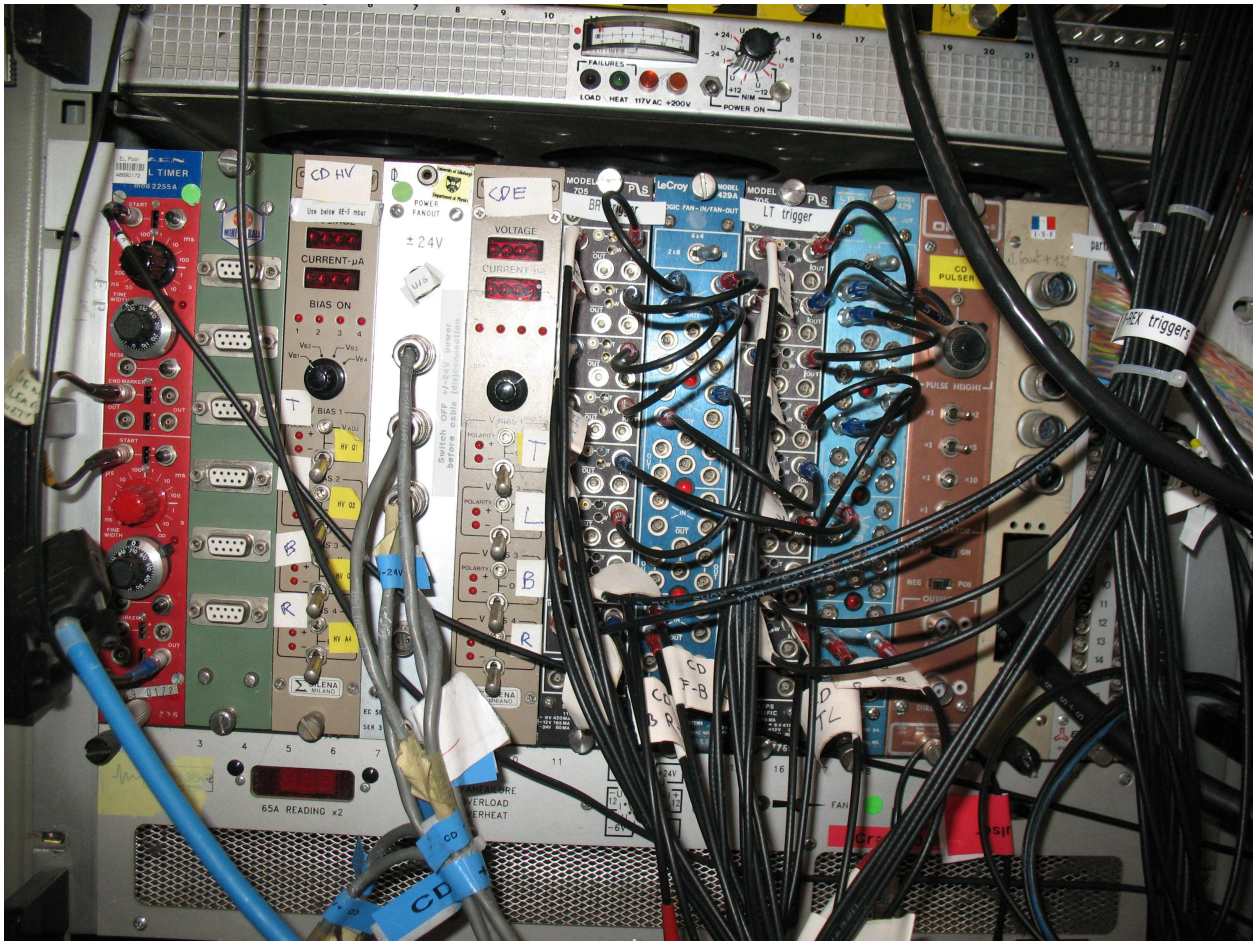

Figure 32: R1.C4: NIM crate - various modules for CD power etc.

31.1.4 NIM crate R1.C5

The first four slots are for the ionisation chamber.

- Slot 1-2 - Emetron dual amplifier “Gas”, “Si”
- Slot 3-4 - Ortec 454 TFA “Gas”
- Slot 5-6 - Slot seems to be broken
- Slot 7-8 - LeCroy 4608C discriminator “unused”, “unused”, “unused”, “unused”, “unused”, “unused”, “unused”, “Ionisation chamber gas”
- Slot 9-22 empty
- Slot 23-24 - laser control box

31.2 Rack 2

In rack 2 we have two crates for the RAL 109 modules with their power supplies and the new DAQ computer pcepuis16 with its RAID array. The NIM crate which was previously in the place now occupied by the DAQ computer is now in R1.C4.

31.2.1 KM-6 crate R2.C1

- Slot 1 - RAL 109 s/n 70 (annular strips)
- Slot 2 - RAL 109 s/n 71 (annular strips)
- Slot 3 - RAL 109 s/n 72 (annular strips)
- Slot 4 - RAL 109 s/n 73 (annular strips)
- Slot 5 - RAL 109 s/n 74 (annular strips)

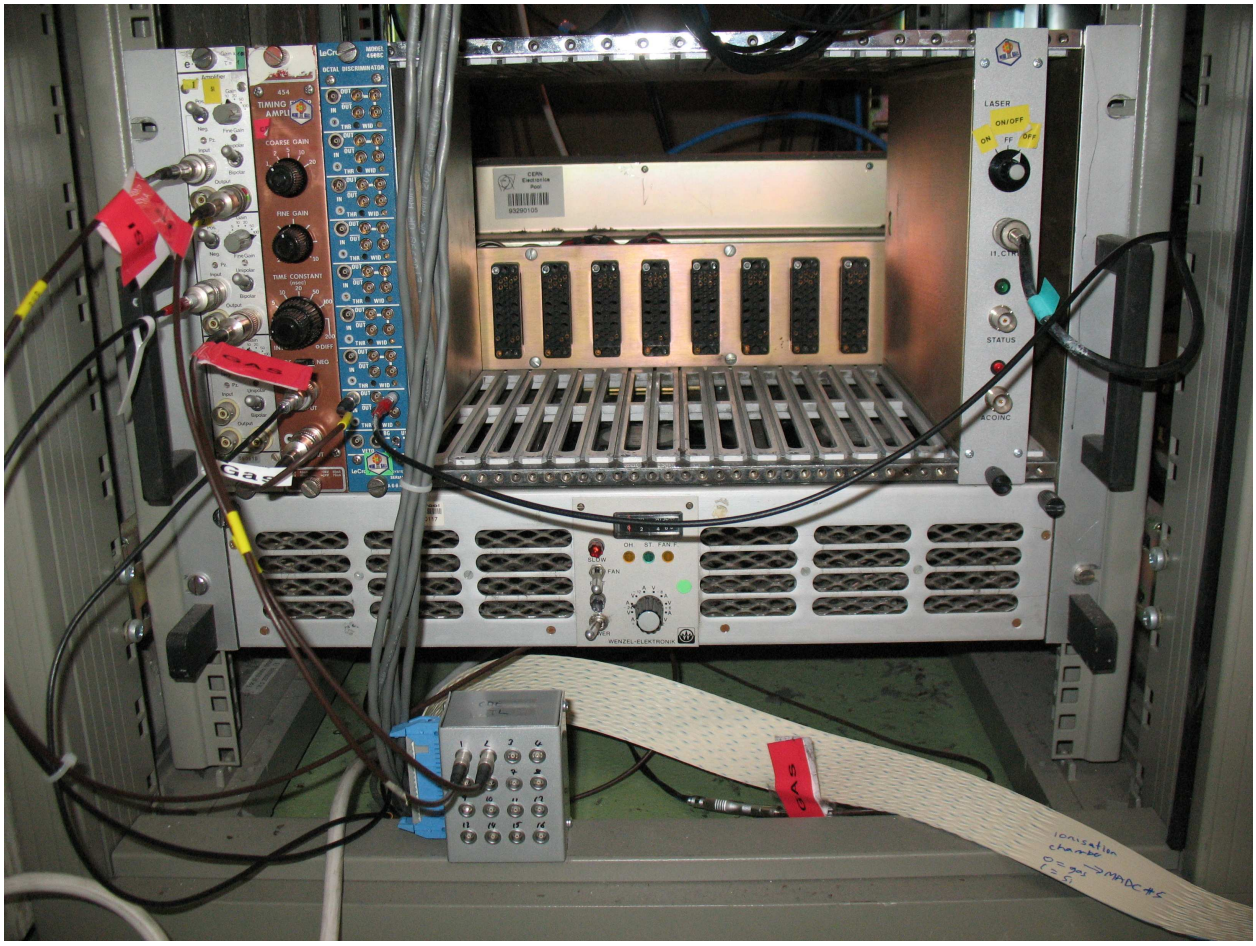

Figure 33: R1.C5: NIM crate - ionisation chamber, laser

- Slot 6 - RAL 109 s/n 75 (annular strips)
- Slot 7 - RAL 109 s/n 76 (annular strips)
- Slot 8 - RAL 109 s/n 77 (annular strips)
- Slot 10 - RAL 109 s/n 91 (PAD detector)

31.2.2 KM-6 crate R2.C2

- Slot 1 - RAL 109 s/n 78 (sector strips)
- Slot 2 - RAL 109 s/n 79 (sector strips)
- Slot 3 - RAL 109 s/n 80 (sector strips)
- Slot 4 - RAL 109 s/n 81 (sector strips)
- Slot 5 - RAL 109 s/n 82 (sector strips)
- Slot 6 - RAL 109 s/n 83 (sector strips)
- Slot 7 - RAL 109 s/n 84 (sector strips)
- Slot 8 - RAL 109 s/n 85 (sector strips)
- Slot 9 - RAL 109 s/n 86 (sector strips)
- Slot 10 - RAL 109 s/n 87 (sector strips)
- Slot 11 - RAL 109 s/n 88 (sector strips)
- Slot 12 - RAL 109 s/n 89 (sector strips)
- Slot 15 - RAL 109 s/n 90 (unused)

Figure 34: R2.C1: The RAL109s for the front rings. The upper connections are for the energy and they are joined up in pairs and sent to the ADC. The lower connections are for the timing and they go to the MALU in R1.C2 and from there to the TDCs in R3.C1.

31.2.3 New DAQ computer and raid array R2.C3

31.2.4 CD connectors and power supplies

At the back of rack 2 we have various connectors and power supplies for the CD detector.

31.3 Rack 3

In rack 3 we have a VME crate and three high-power NIM crates.

31.3.1 VME crate R3.C1

- Slot 1 - power PC
- Slot 2 - VME trigger module
- Slot 3 - Mesytech MADC32 (CD E Q1) 0x00F10000
- Slot 4 - Mesytech MADC32 (CD E Q2) 0x00F30000
- Slot 5 - Mesytech MADC32 (CD E Q3) 0x00F40000
- Slot 6 - Mesytech MADC32 (CD E Q4) 0x00F50000
- Slot 7 - CAEN V775 TDC (CD T Q1) 0x00F70000
- Slot 8 - CAEN V775 TDC (CD T Q2) 0x00F80000
- Slot 9 - CAEN V775 TDC (CD T Q3) 0x00F90000
- Slot 10 - CAEN V775 TDC (CD T Q4) 0x00FA0000
- Slot 11 - Mesytech ADC (ionisation chamber) 0x00F60000

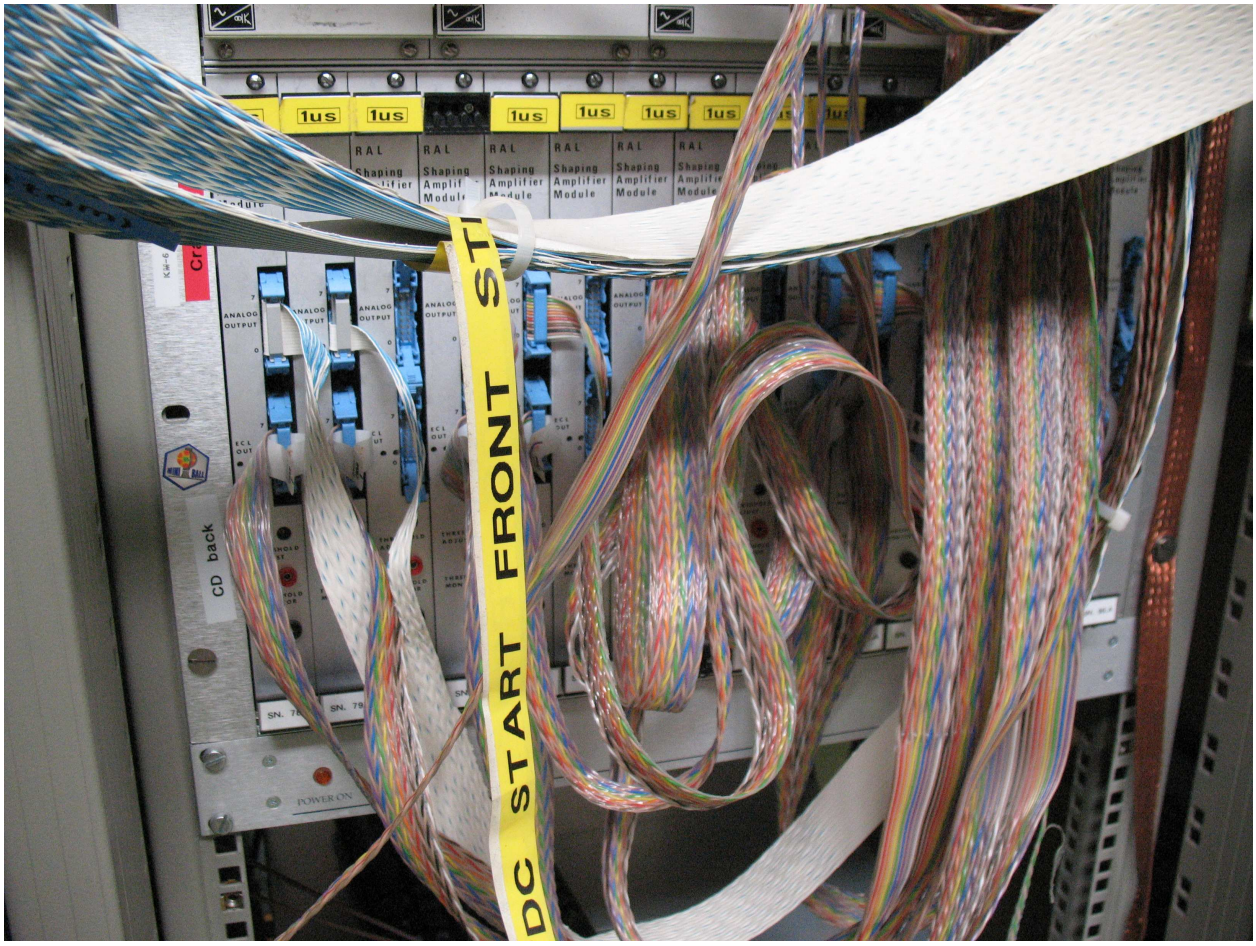

Figure 35: R2.C2: The RAL109s for the back sectors. The upper connections are for the energy and they are joined up in pairs and sent to the ADC. Note that the first pair has the blue and white cable on to which the signal for laser power is added. The lower connections are for the timing and they go directly to the TDC in R3.C1

- Slot 12 - blank
- Slot 13 - pattern unit 0x00303800
- Slot 14 - scaler with NIM inputs 0x00302800
- Slot 15 - scaler with ECL inputs (PPAC X) 0x00300800
- Slot 16 - scaler with ECL inputs (PPAC Y) 0x00301800
- Slot 17 - Wiener VC32 (CAMAC 1) 0x00550000
- Slot 18 - Wiener VC32 (CAMAC 2) 0x00558000
- Slot 19 - Wiener VC32 (CAMAC 3) 0x00560000
- Slot 20 - SiS 3300 100 MHz 12 bit ADC (Bragg Detector) 0x40000000
- Slot 21 - VDIS

31.3.2 NIM crate R3.C2

- Slot 1-6 - TB8000 trigger box (triple width) “Trigger box”
- Slot 7-8 - CAEN N454 4x4 fan-in/fan-out “Delay trg Q1…4”
- Slot 9-10 - LeCroy 370C strobed coinc “coinc PG1…4”, “four channels unused”
- Slot 11-12 - CAEN N455 quad coinc logic “Q1…4 coinc or downscaled”
- Slot 13-14 - LeCroy 465 triple coinc unit “DGF Synch or ADC busy for Q1…3”

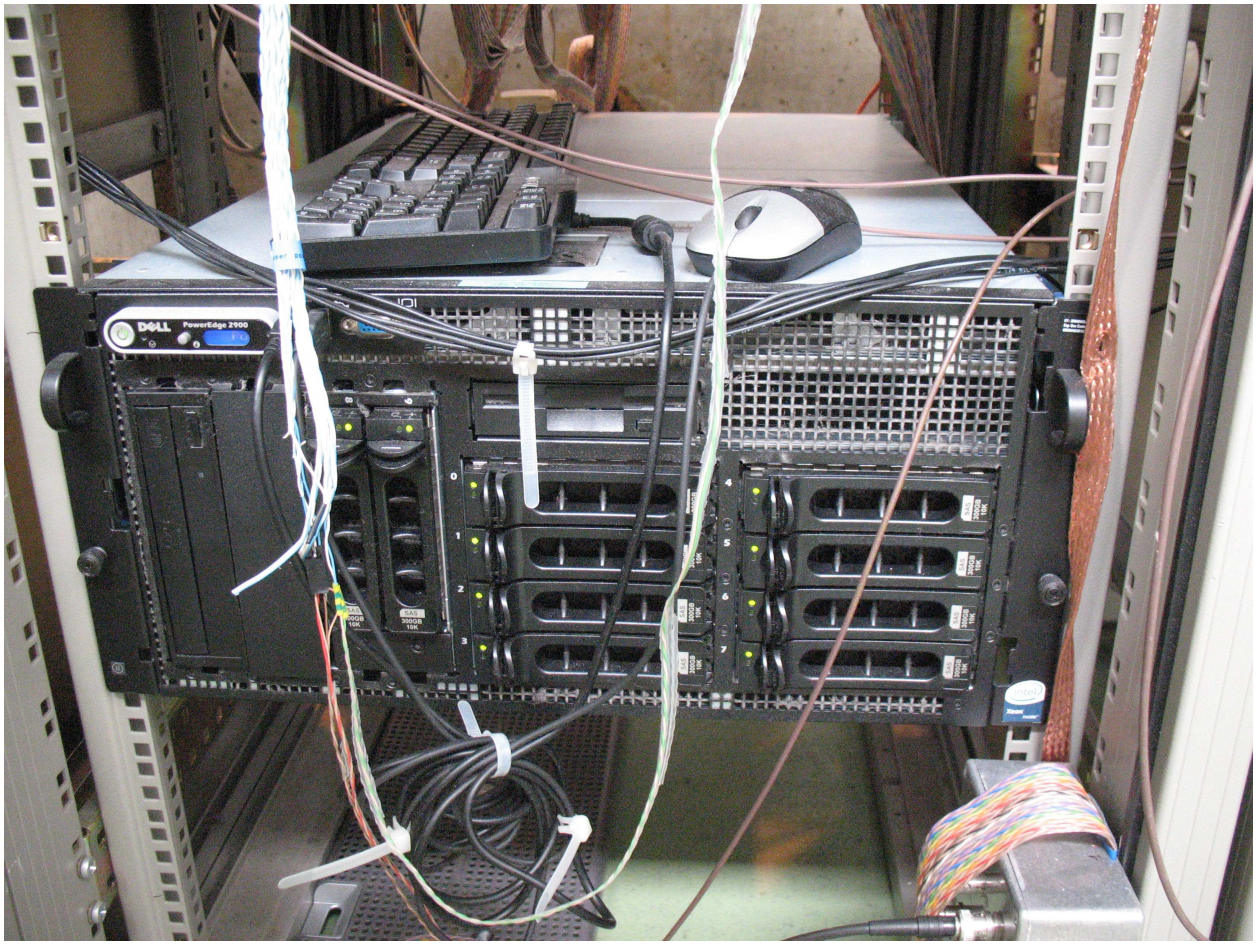

Figure 36: R2.C3: The new DAQ computer and raid array

- Slot 15-16 - LeCroy 465 triple coinc unit “DGF Synch or ADC busy for Q4”, “DAQ trig if DAQ not busy”, “Ionisation chamber”
- Slot 17-18 - GG8000 octal gate generator “Q1...4 ADC/TDC gate”, “Ionisation chamber”, “Bad”, “DAQ trigger”, “γ OR”
- Slot 19-20 - LeCroy 429A 4x4 fan-in/fan-out “Q1...4 ADC/TDC gate”
- Slot 21-22 - IKP modified TFA (in Ortec housing) “Mult out”
- Slot 23-24 - CAEN N454 2x8 fan-in/fan-out “Gamma Or”, “Si OR”

31.3.3 NIM crate R3.C3

- Slot 1-2 - TTL/NIM → ECL converter (set to NIM) “DAQ Trigger”
- Slot 3-4 - ECL → TTL/NIM converter (set to NIM) “unused”, “unused”, “unused”, “unused”, “DAQ dead”, “DAQ Go”
- Slot 5-6 - LeCroy 429A 4x4 fan-in/fan-out “ADC busy or SYNCH 1... 4”
- Slot 7-8 - Noname dual timer “Delay Q1 (both parts)”
- Slot 9-10 - CAEN N93B dual timer “Delay Q2 (both parts)”
- Slot 11-12 - Noname dual timer “Delay Q3 (both parts)”
- Slot 13-14 - CAEN N93B dual timer “Delay Q4 (both parts)”
- Slot 15-16 - LeCroy 429A 4x4 fan-in/fan-out “Q1...4 trigger”
- Slot 17-18 - LeCroy 429 2x8 fan-in/fan-out “MADC clock”, “MADC reset”
- Slot 19-20 - LeCroy 465 triple coincidence unit “1 MHz and laser on”, Ion and not DAQ dead”, “1s and EBIS”

Figure 37: R2.rear: +/-15 Volt power supply for the CD preamps

- Slot 21-22 - CAEN 2255A Dual Timer “DAQ dead extend”, “1s in EBIS”
- Slot 23-24 - CAEN N454 4x4 fan-in/fan-out “DAQ dead”, “DAQ dead+”, “DAQ dead+”, “1s in EBIS”

Note the first module is for signals going to the DAQ and the second for signals coming from the DAQ. Originally, the first four channels of the second module were the ADC busy signals for the four CAEN ADCs, which had to be converted from ECL to NIM, but the Mesytec MADC-32s provide a NIM signal directly, so they are no longer used.

31.3.4 NIM crate R3.C4

- Slot 1-2 - TTL → NIM and NIM → TTL converter “EBIS pulse”, “PS”, “T1”
- Slot 3-4 - ISOLDE 1Hz-1MHz clock
- Slot 5-6 - LeCroy 429A 4x4 fan-in/fan-out “Laser off”, “1 MHz”, “not used”, “GFLT”
- Slot 7-8 - CAEN N455 quad coinc logic “T1 AND DGF busy”, “1 MHz and on win”, “1 MHz and on/off”, “DGF busy and PS start”
- Slot 9-10 - Noname dual timer “Delayed TS PS start”, “PS del”
- Slot 11-12 - CAEN 2255B dual timer “unused”, “direct TS PS start”
- Slot 13-14 - CAEN 2255B dual timer “MADC reset”, “MADC reset width”
- Slot 15-16 - CAEN N454 4x4 fan-in/fan-out “T1”, “start PS cycle”, “DGF busy”, “10 μs after DGF not busy”
- Slot 17-18 - CAEN N93B dual timer “T1 veto”, “TS delay”
- Slot 19-20 - CAEN 2255B dual timer “10 μs del”, “something bizarre!”
- Slot 21-22 - Phillips quad linear fan-in/fan-out “unused”, “T1 not busy”, “PS TS”, “unused”

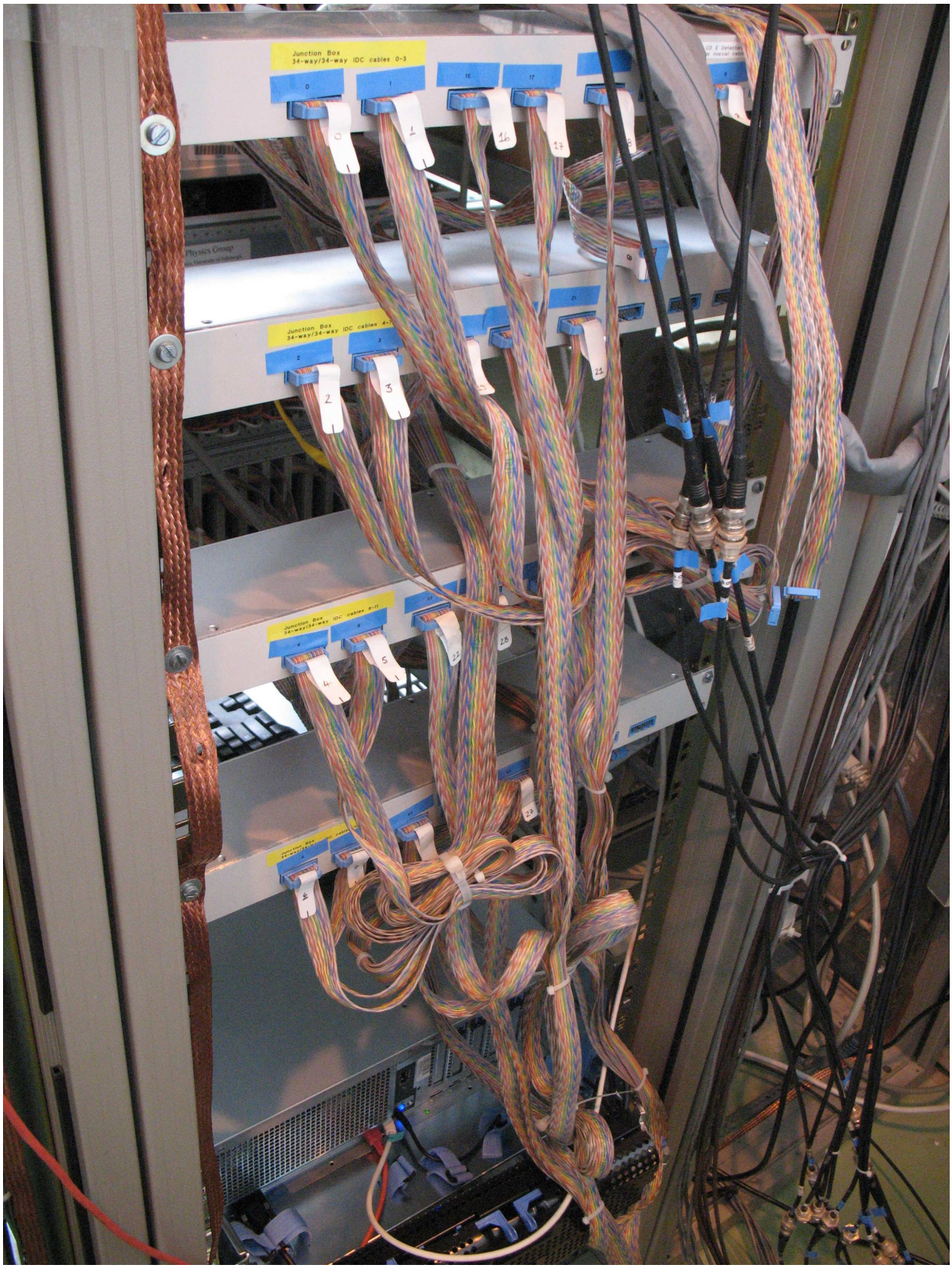

Figure 38: R2.rear: various CD connectors and power supplies

- Slot 23-24 - CAEN 2255B dual timer “TS gate T1”, “TS gate T1 delay”

The last part of the module in slots 19-20 is rather odd. It has as input, the GFLT and then it sends its output to the level converter in slot 1-2 to convert it to TTL and from there it goes to the analog fan-out in R1.C3.S3-4 and then two outputs go from there, over the wall to the Miniball target chamber area, where they just hang. Presumably they were something to do with the diamond detector, the tilted foil experiment or T-REX.

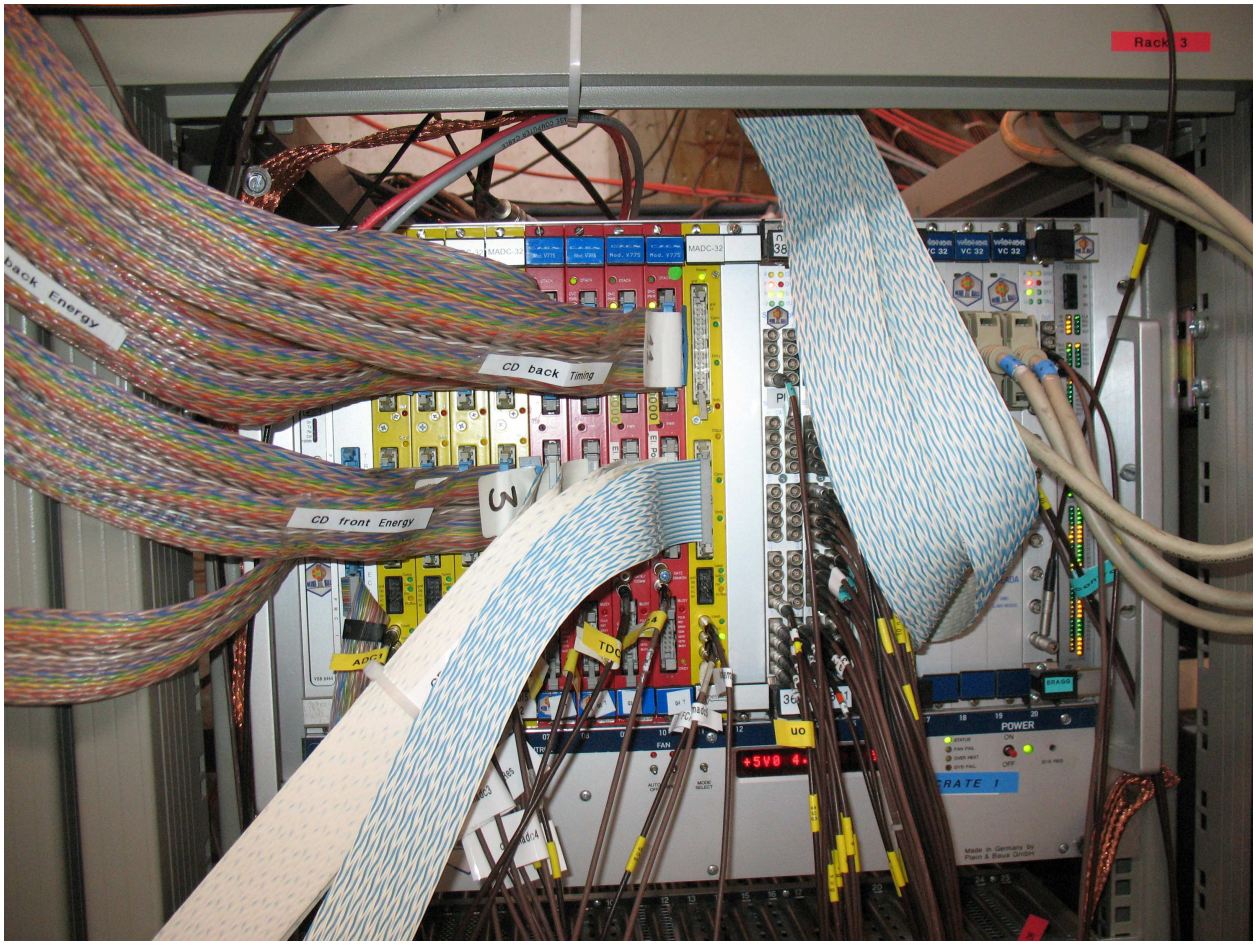

Figure 39: R3.C1: The cabling of the CD to the VME ADCs and TDCs. The four ADCs are the left yellow modules and the four TDCs are the next four red ones. The front signals use the lower parts of the ADCs and TDCs and the back signals use the upper parts. Also shown is the bunch of LEMO cables for the scalers, the pair of blue and white flat cables for the PPAC and the SCSI cables for the VC32→CC32 connection

31.3.5 Preamp power - R3 rear

At the back of rack 3, we have the preamp power for the Miniball detectors and possibly PPAC and beam-dump detector preamp power. Note that this module only supplies ± 12 Volts. (Some detectors may require ± 24 Volts as well and cannot be used with this power supply).

This power supply is in two parts, the power supply itself (like that for a crate) and the distribution panel with a row of D-sub connectors.

Note this preamp power supply should be connected to the mains via a dead-man's switch, which switches off if the mains power goes off. So if we have a power failure, the preamp power doesn't automatically come on, but has to be reset manually by pushing the button. The reason for this is that when the power comes back on at CERN after a power outage, there is a huge surge, as all the machines start up, which can damage the warm preamps.

31.4 Rack 4

In rack 4 we have three CAMAC crates and one high-power NIM crate.

31.4.1 CAMAC crate R4.C1

- Slot 3 - XIA DGF 1154
- Slot 4 - XIA DGF 1153
- Slot 5 - XIA DGF 1119
- Slot 6 - XIA DGF 1103
- Slot 7 - XIA DGF 1101

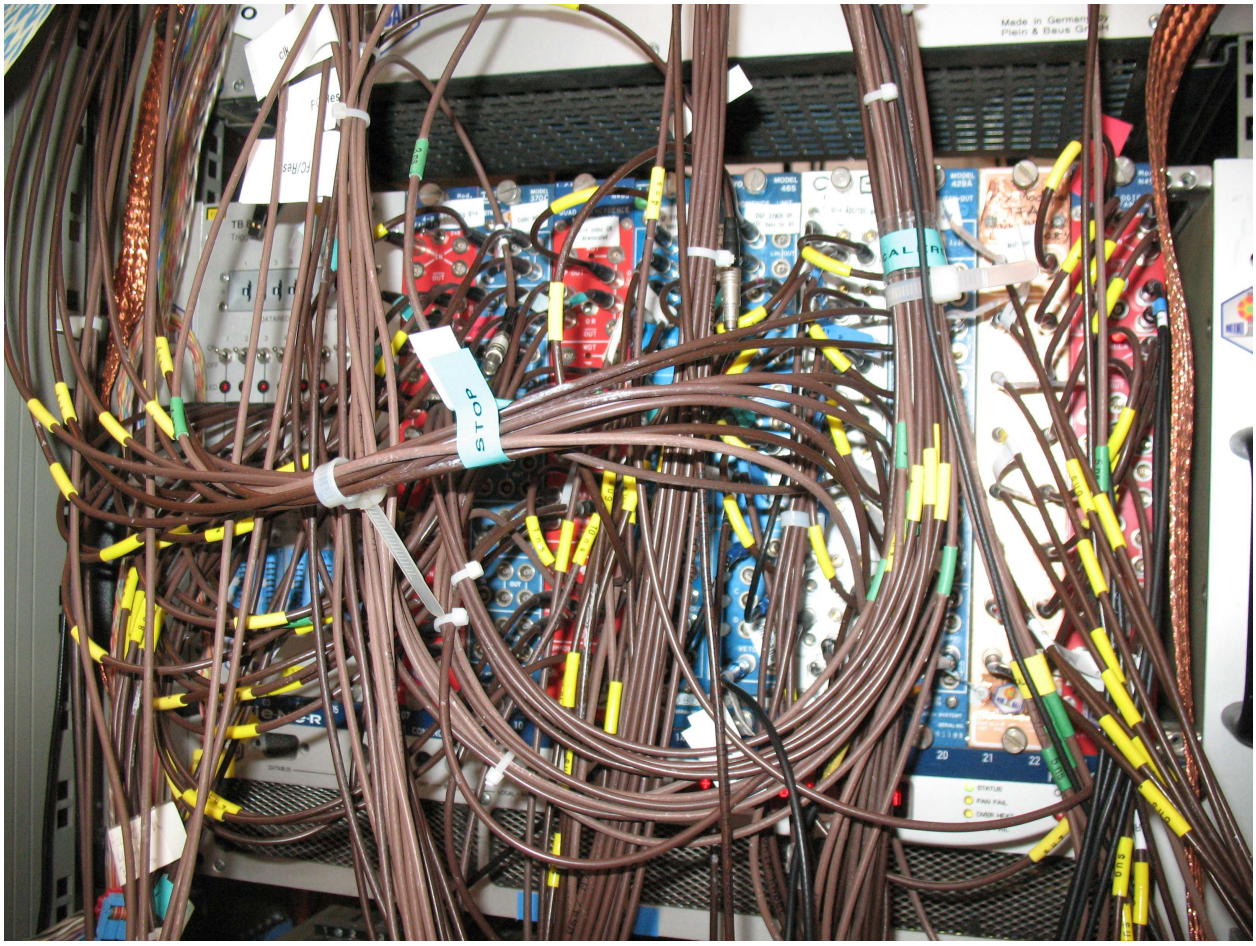

Figure 40: R3.C2: NIM crate - mostly trigger logic. Note that the two LEMO cables hanging down in the picture are the 40 MHz clock and fast reset for the sixth MADC32, which isn't present in this setup.

- Slot 8 - XIA DGF 1148
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1158
- Slot 11 - XIA DGF 1107
- Slot 12 - XIA DGF 1163
- Slot 13 - XIA DGF 1139
- Slot 14 - XIA DGF 1162
- Slot 15 - XIA DGF 1161
- Slot 16 - XIA DGF 1120
- Slot 17 - XIA DGF 1166
- Slot 18 - XIA DGF 1194
- Slot 19 - XIA DGF 1184
- Slot 20 - XIA DGF 1122
- Slot 21 - XIA DGF 1174
- Slot 24-25 Wiener CC32

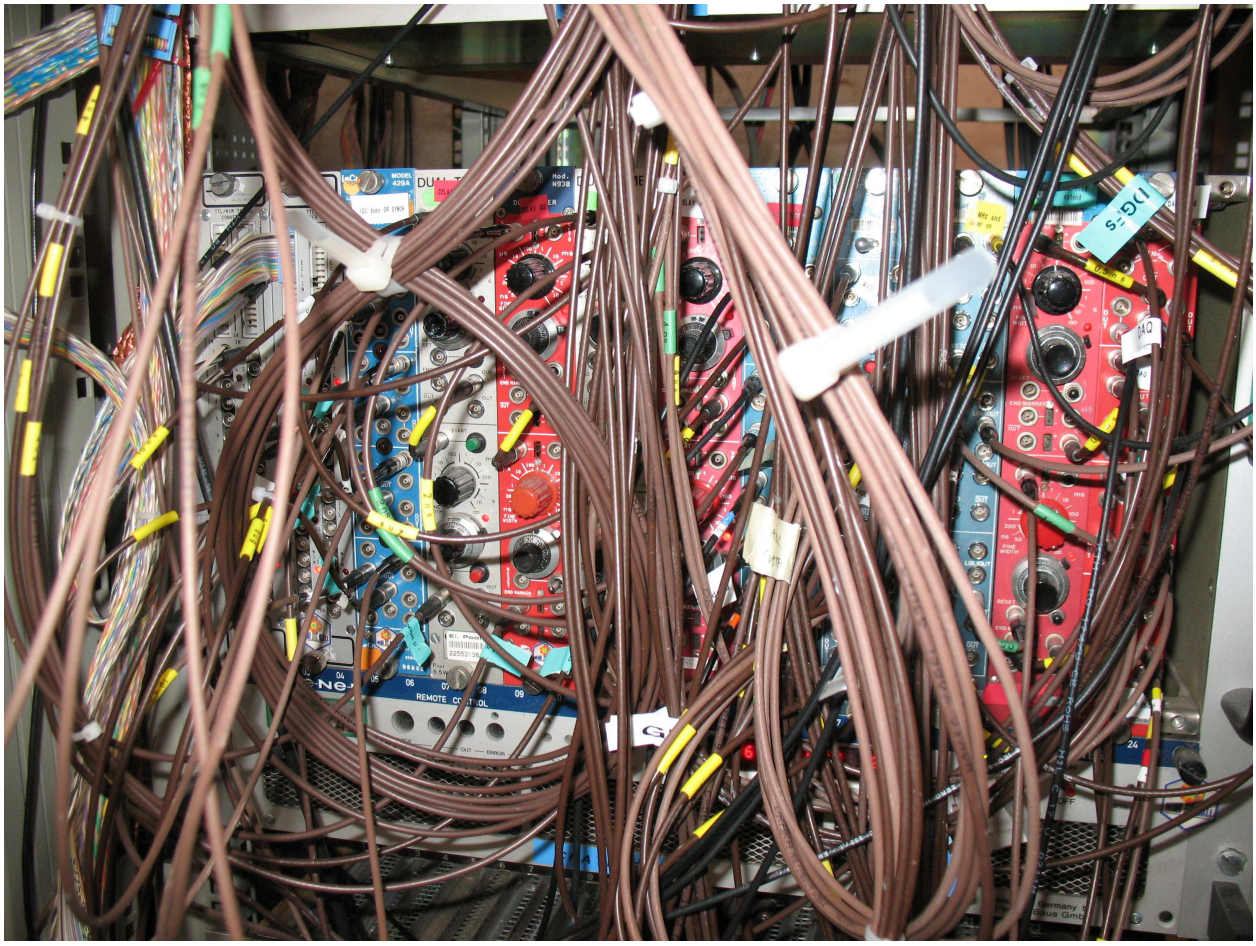

Figure 41: R3.C3: NIM crate - mostly trigger logic

31.4.2 CAMAC crate R4.C2

- Slot 3 - XIA DGF 1176
- Slot 4 - XIA DGF 1175
- Slot 5 - XIA DGF 1159
- Slot 6 - XIA DGF 1171
- Slot 7 - XIA DGF 1106
- Slot 8 - XIA DGF 1100
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1108
- Slot 11 - XIA DGF 1190
- Slot 12 - XIA DGF 1152
- Slot 13 - XIA DGF 1167
- Slot 14 - XIA DGF 1113
- Slot 15 - XIA DGF 1104
- Slot 16 - XIA DGF 1130
- Slot 17 - XIA DGF 1123
- Slot 18 - XIA DGF 1192
- Slot 19 - XIA DGF 1138

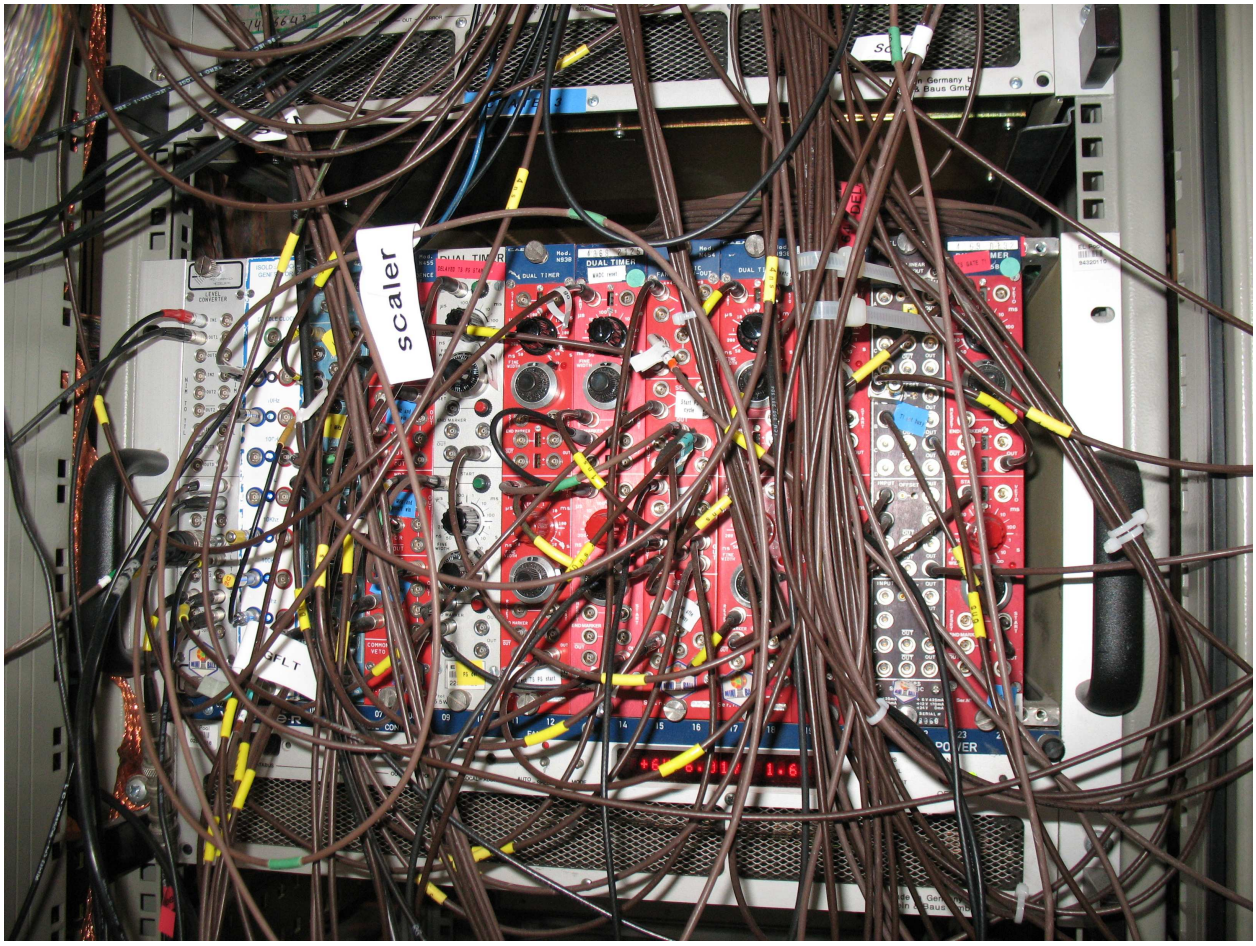

Figure 42: R3.C4: NIM crate - mostly PS and T1 signals.

- Slot 20 - XIA DGF 1128
- Slot 21 - XIA DGF 1147
- Slot 24-25 Wiener CC32

31.4.3 R4.C3

- Slot 4 - XIA DGF 1132 “Q1 timestamp”
- Slot 5 - XIA DGF 1178 “Q2 timestamp”
- Slot 6 - XIA DGF 1149 “Q3 timestamp”
- Slot 7 - XIA DGF 1137 “Q4 timestamp”
- Slot 8 - XIA DGF 1142 “EBIS”, “T1”,”PS”
- Slot 9 - XIA DGF 1189 “Beam dump”, “unused”,“unused”
- Slot 10 - IKP 40 MHz clock
- Slot 11 - XIA DGF 1124
- Slot 12 - XIA DGF 1170
- Slot 13 - XIA DGF 1129
- Slot 14 - XIA DGF 1169
- Slot 15 - XIA DGF 1151
- Slot 16 - XIA DGF 1150
- Slot 17 - XIA DGF 1145

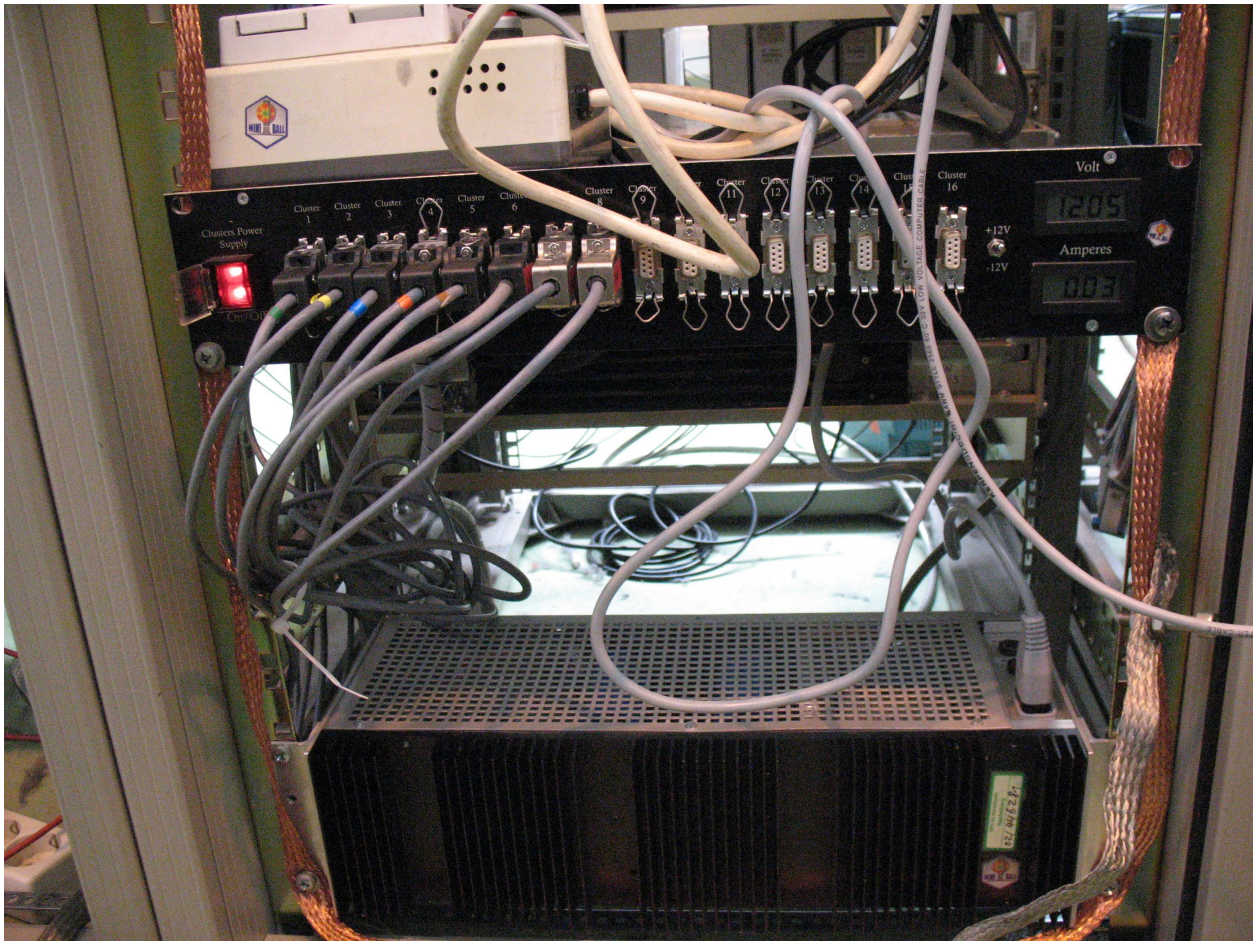

Figure 43: R3.rear: Preamp power supply and distributor

- Slot 18 - XIA DGF 1118
- Slot 19 - XIA DGF 1134
- Slot 20 - XIA DGF 1181
- Slot 21 - XIA DGF 1186
- Slot 22 - XIA DGF 1109
- Slot 24-25 Wiener CC32

Note that module 1181 is in slot 20 not 1193 which was there in previous years, because the last channel of 1193 is broken.

31.4.4 NIM crate R4.C4

- 1-2 - CAEN N93B dual timer "Force readout", "DAQ trigger"
- 3-4 - CAEN N93B dual timer "EBIS", "Max on/off window"
- 5-6 - CAEN N454 2x8 fan-in/fan-out "EBIS pulse", "GFLT"
- 7-8 - LeCroy 365AL 4-fold logic unit "DAQ crash reset", "End RDO and in time"
- 9-10 - CAEN N93B dual timer "TDGF Ebis", "Off window"
- 11-12 - CAEN 2255B dual timer "Not busy", "End RDO"
- 13-14 - IKP 3 fan-in/39 fan-out "GFLT"
- 15-16 - IKP 3 fan-in/39 fan-out "GFLT"
- 17-18 - IKP 3 fan-in/39 fan-out "Synch"

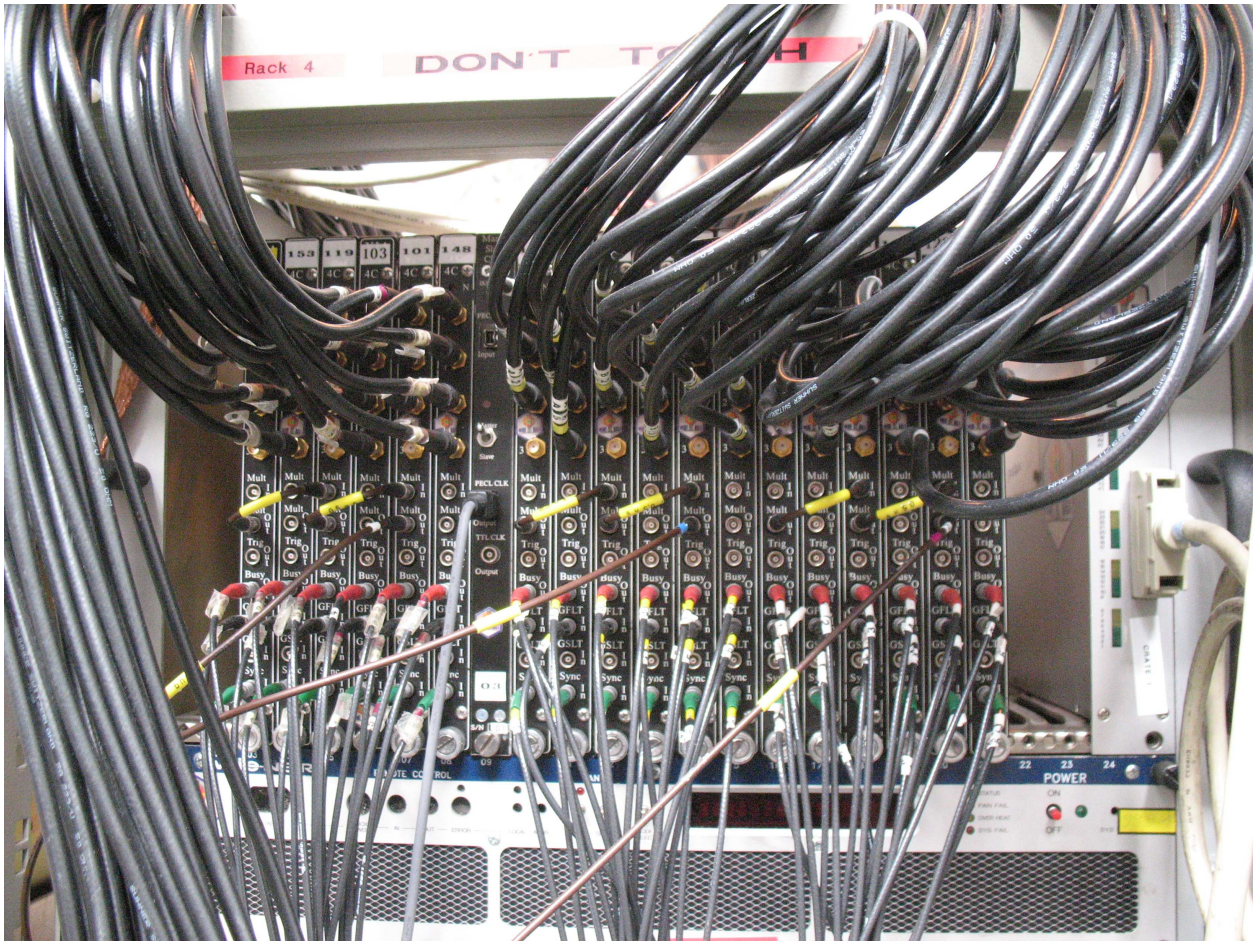

Figure 44: R4.C1: CAMAC crate of DGFs for three clusters.

- 19-20 - IKP 3 fan-in/39 fan-out "Synch"
- 21-22 - IKP 39 fan-in/3 fan-out "Busy"
- 23-24 - IKP 39 fan-in/3 fan-out "Busy"

31.5 Rack 5

Rack five contains (from top to bottom) the old PT100 box, the filling computer monitor, the old filling computer (pcepsc22), its keyboard, the PT100 box, the four manifold controller boxes (with box D highest), raid array, old DAQ computer (pcepuis20), CAEN HV power supply and UPS.

Note that there are now two filling systems. The old filling computer (pcepsc22) is connected to the old PT100 readout and can be connected to the manifolds in place of the new system. In the photograph, the new system is connected (i.e. the PT100s from the detectors go to the new PT100 box and the manifolds are controlled by the new USB based system. The old DAQ computer (pcepuis20) is being used as the filling computer. It is connected to the USB digital I/O for manifold control and the new PT100 readout via a USB hub.

31.5.1 Autofill connections - R5 rear

31.5.2 HV connections - R5 rear

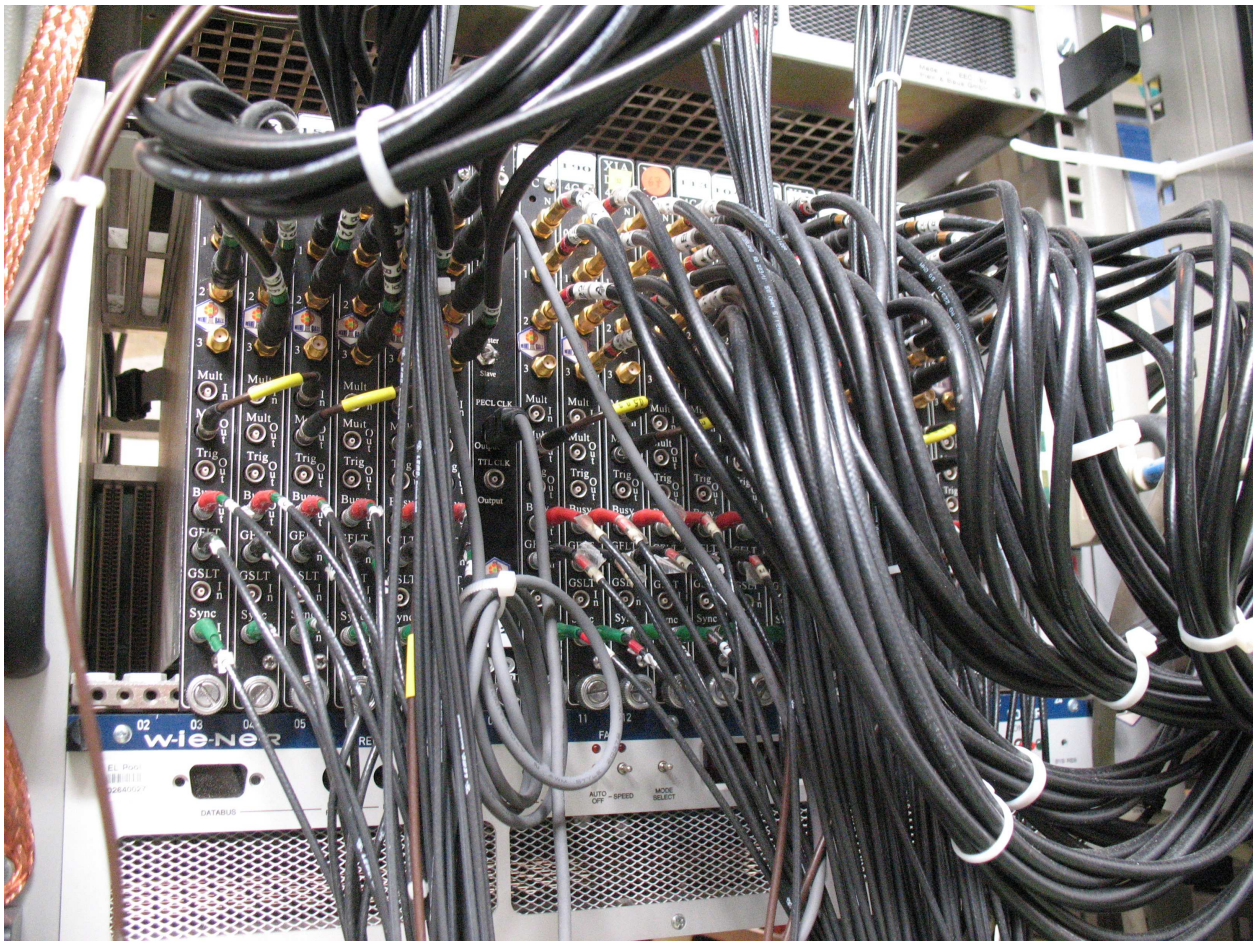

Figure 45: R4.C2: CAMAC crate of DGFs for three clusters.

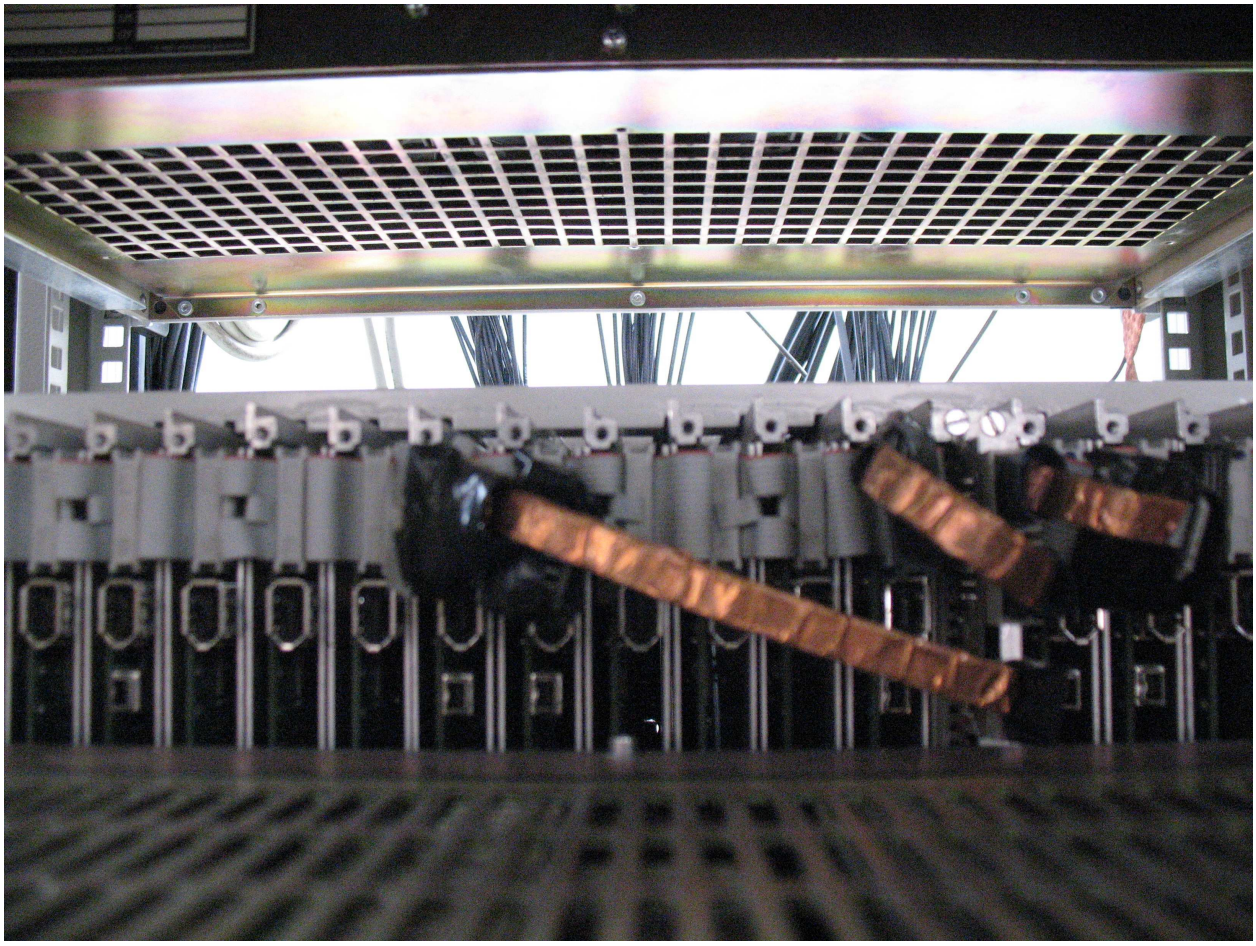

Figure 46: R4.C2: The rear of the DGFs showing the backplane bus connection. Each flat cable with 8 connectors has a terminator resistor block, six DGFs and the connector to the 40 MHz clock module. The trigger lines between DGFs associated with different capsules are cut, while those for each pair of DGFs handling a single capsule are connected.

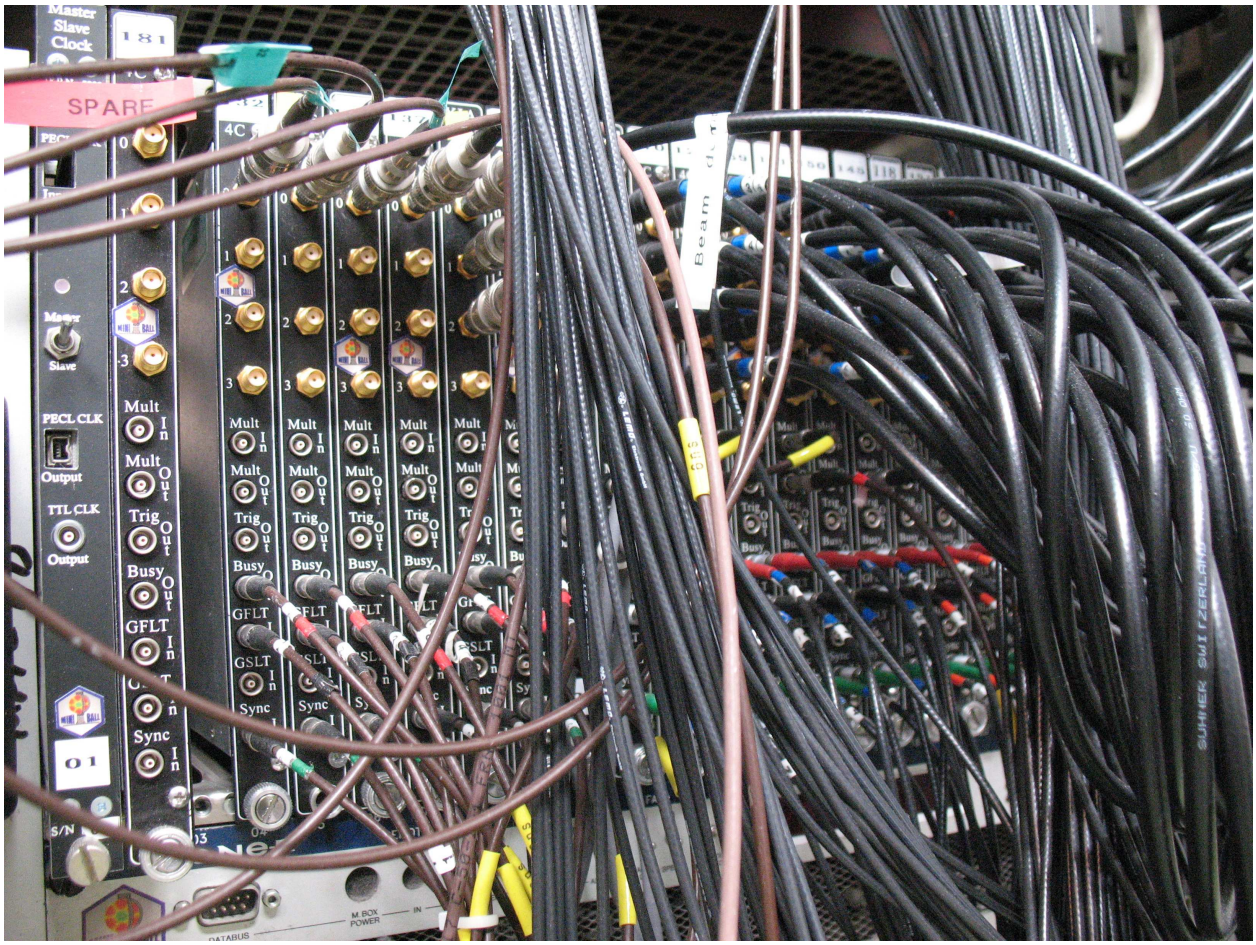

Figure 47: R4.C3: CAMAC crate of DGFs. Note the left four are the timestamper DGFs, then there is the EBIS etc. DGF and the sixth DGF is for the beam dump detector.

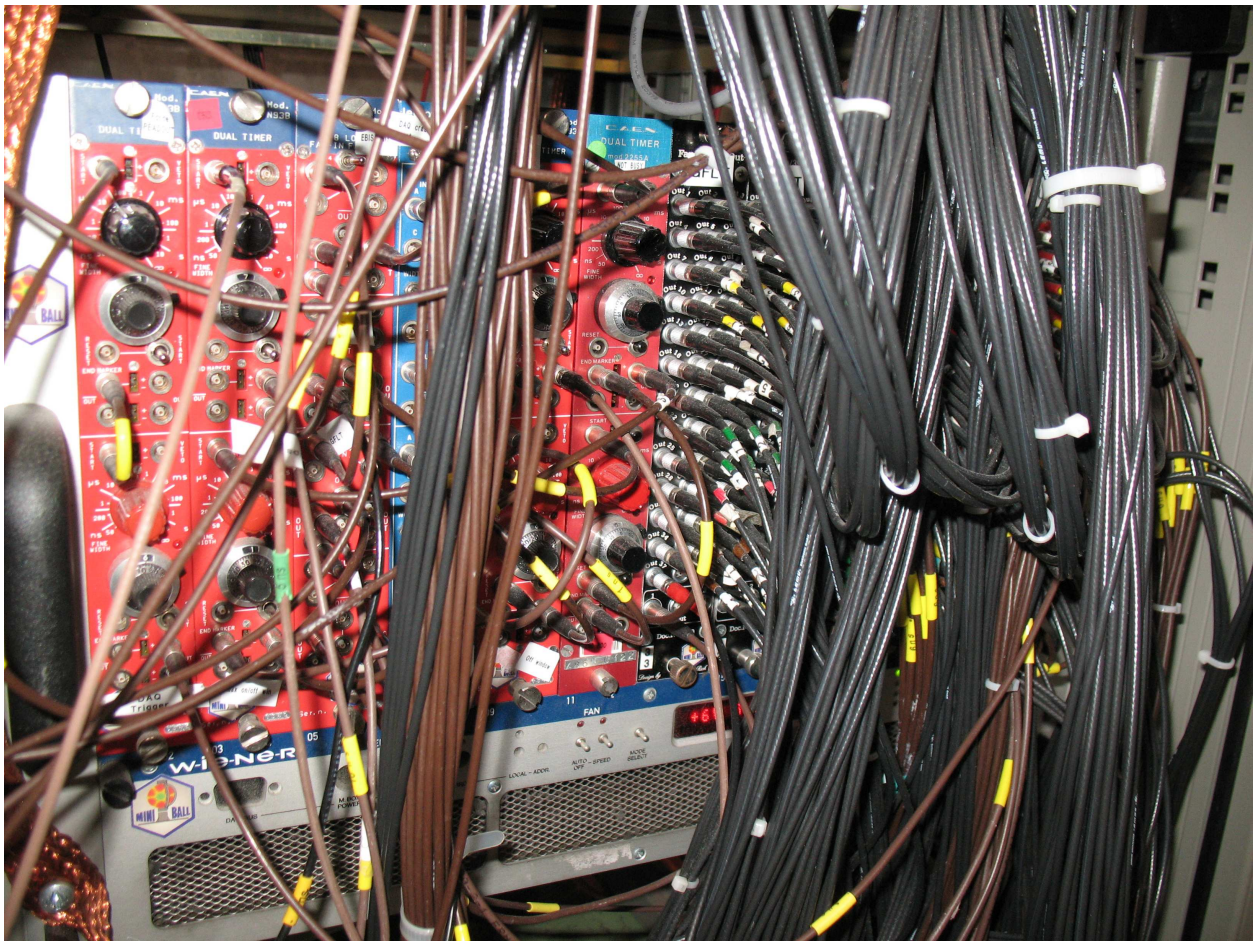

Figure 48: R4.C4: NIM crate

Figure 49: R5 bottom: filling system computer with monitor and keyboard, new PT100 box and four manifold controller boxes, raid array, DAQ computer, CAEN HV power supply and UPS. The old PT100 box is above the monitor.

Figure 50: R5 rear: autofill connectors

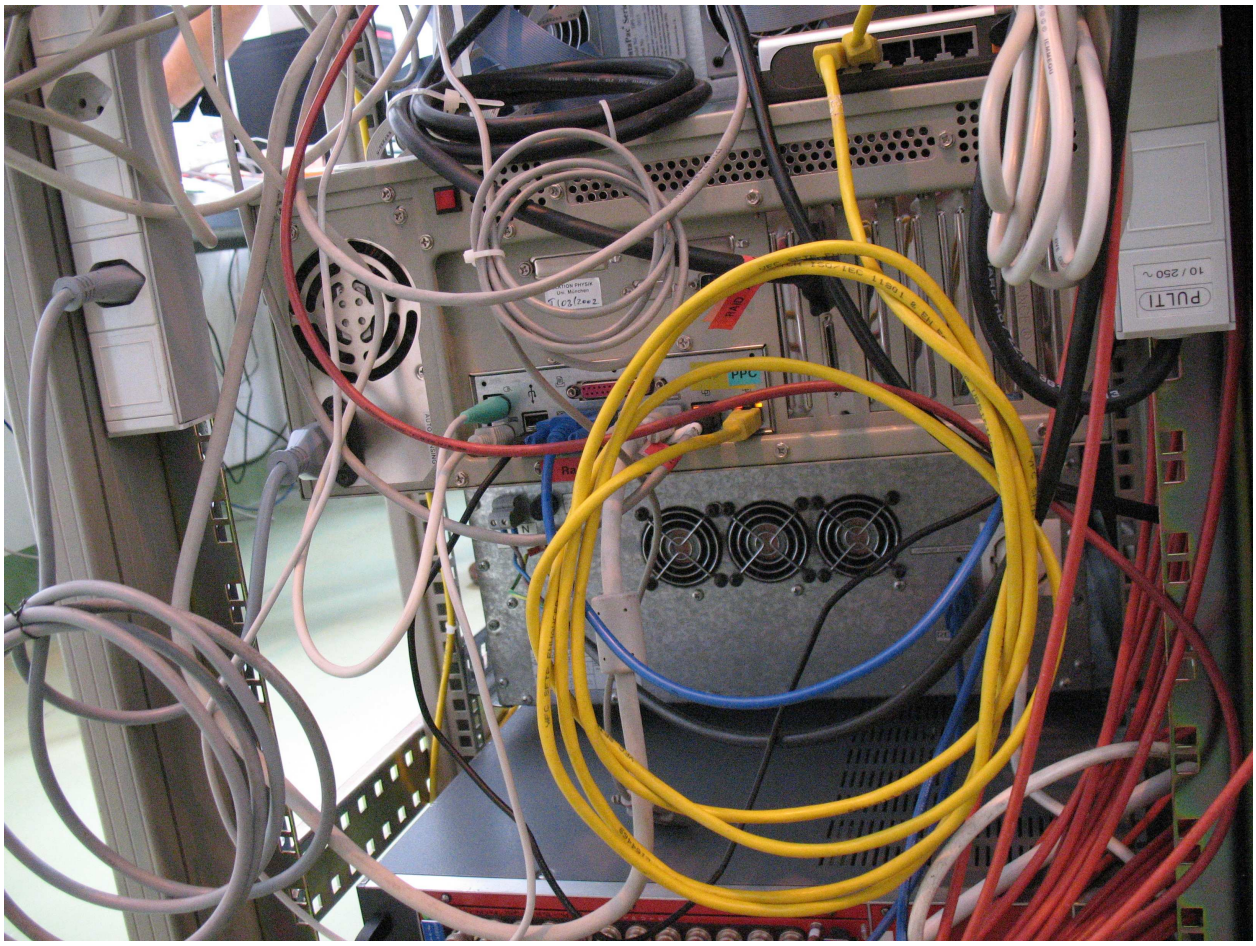

Figure 51: R5 rear: autofill connectors

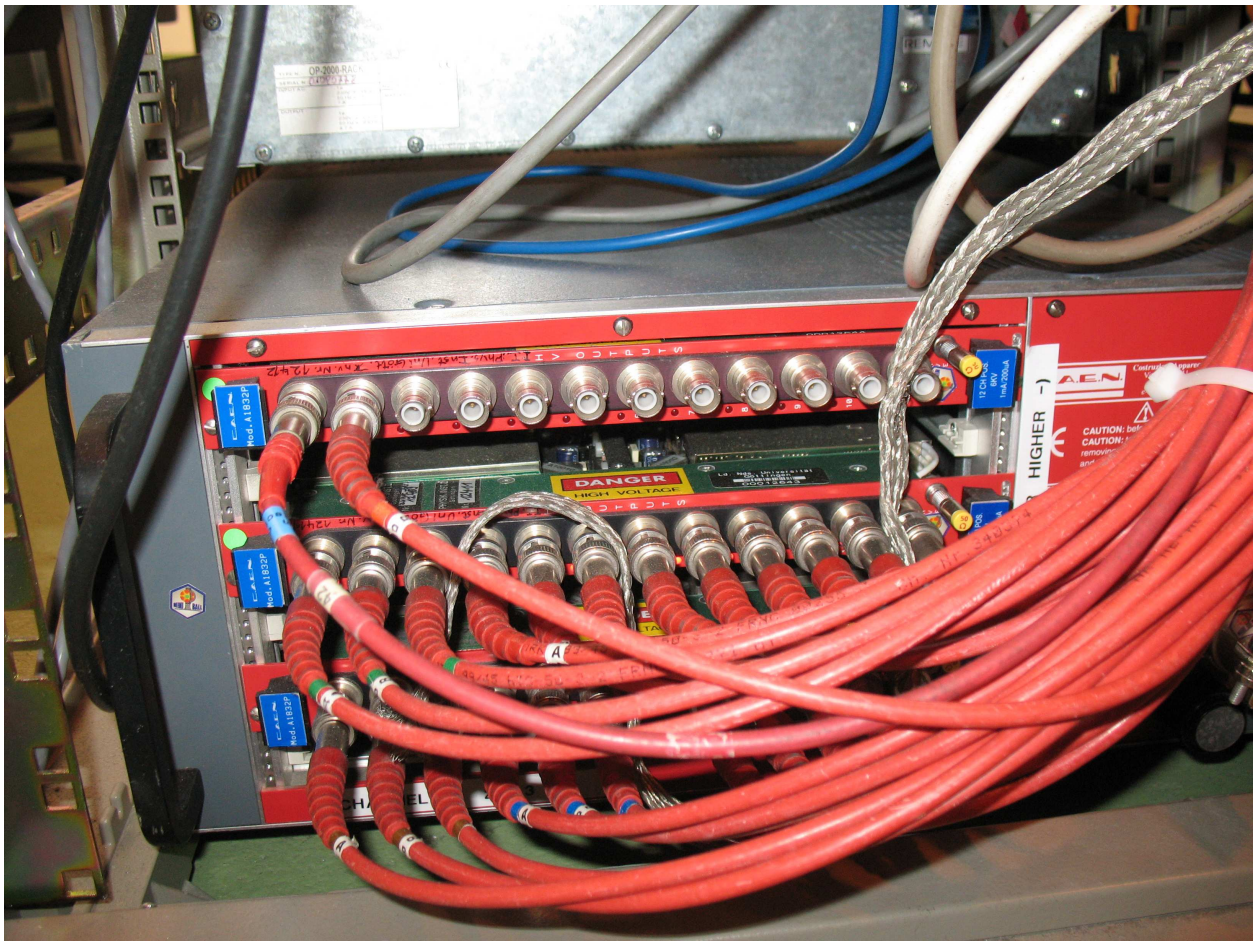

Figure 52: R5 rear: HV connectors