Miniball electronics at CERN

Contents

[1] Nigel Warr September 2003

1 Foreword

This document describes the state of the electronics used at CERN for the September experiment. That means it is different to all previous experiments and is likely to be different to future ones. However, there should be certain similarities.

The electronics for this setup has grown gradually rather than being thought out as a single setup, so modules were not necessarily placed in the optimal position in the crates. In places, signals were duplicated due to different people building different parts of the setup and not realising that the signal they were constructing was already available. In other places, conditions have been applied to signals which can only be generated if the condition is satisfied, so that the condition was superfluous.

However, the setup works, so there is no reason to change it!

Caveat: this document was produced during experiments with all the interruptions that that entails, so it probably contains mistakes. Use it with caution!

2 The discriminated Si trigger

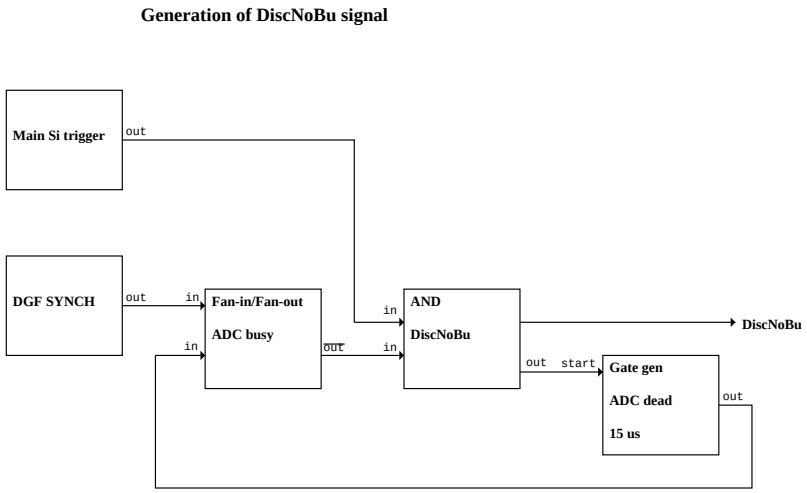

Figure 1: The generation of the DiscNoBu signal

The signal labelled **DiscNoBu** is the main Si trigger discriminated by the ADC not busy condition. The feedback is to block all subsequent events which

occur during the busy time of the ADC. Note that we do not take the real BUSY signal from the ADC which is an ECL signal, but simply start a gate at the same time as the ADC gate and lasts for 15 μs. This is used to prevent acceptance of further Si triggers during those 15 μs. Note that we originally set a value of 15 μs which we were sure was long enough to be at least as long as the real ADC busy. Later, we looked at this artificial busy and the real busy on the scope and shortened the time of this artificial busy to match the real one. Heiko Scheit says this is wrong and has increased it to 16 μs.

3 Generation of the ADC gate, the TDC common stop and the Timestamper DGF input signal

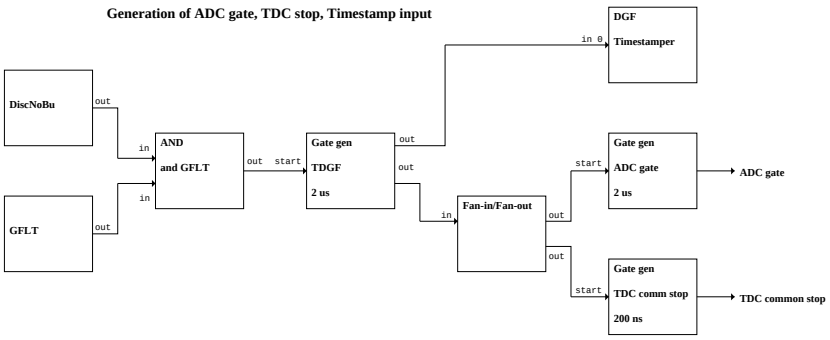

Figure 2: Generation of the ADC gate, the TDC common stop and the timestamper DGF signal from the DiscNoBu signal

The **DiscNoBu** signal is gated by the GFLT. This GFLT signal is the same as the on/off window (i.e. it is open during the EBIS pulse and then again afterwards). In other words, we gate the DGFs with the GFLT and we gate the particle trigger with the GFLT as well.

That gated signal is used to start the **TDGF** signal which is 2 μs long and is fed directly as the input to the timestamper DGF. The output from that module is also passed into a fan-in/fan-out and one part is used to start the ADC gate which is also 2 μs and the other part to generate a stop pulse 200 ns after the Si trigger. Note that both the ADC gate and the TDC common stop are triggered by the leading edge of the gate generator, so they could just as easily have been taken from the AND, except that there were not enough free outputs on the AND.

4 Generation of the DAQ trigger

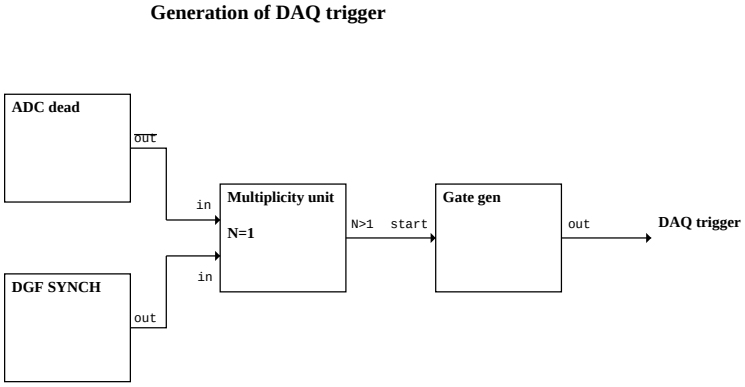

Figure 3: Generation of the DAQ trigger

Normally we want to send a trigger to the MBS to start readout as soon as the DGFs are full. For this we can use the BUSY/SYNCH loop of the DGFs. The first DGF (including the timestamper and the beam dump DGFs) to become full, sets its BUSY and all the BUSY signals are ORed together to generate the SYNCH. We can, therefore, trigger the DAQ when the SYNCH occurs. However, if the ADC is in the middle of a conversion we wish to delay the DAQ trigger until after that conversion. Since the SYNCH remains active until readout occurs, we simply perform an AND between the SYNCH and the inverted ADC dead signal using a multiplicity unit.

If the ADC is not busy, the multiplicity unit's output will become active as soon as the SYNCH becomes active, so the DAQ trigger follows immediately after the SYNCH. If the ADC is busy, the multiplicity unit's output will only change when the ADC is no longer busy.

Note that this is a simplification of the original trigger which took the SYNCH and ORed it with another condition. That other condition was also used to generate a SYNCH so the SYNCH was present anyway. That meant that the OR was superfluous.

5 Generation of the EBIS window

The EBIS window is a 700 μs window which starts when the EBIS gate opens. It is generated using the TTL pulse which comes over from the EBIS platform.

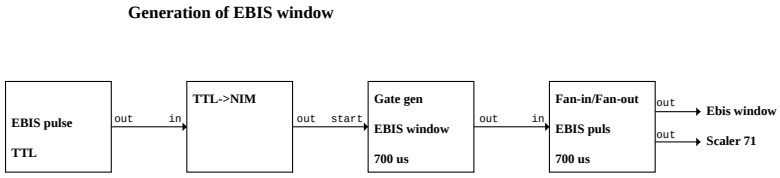

Figure 4: Generation of the EBIS window

6 Generation of off window

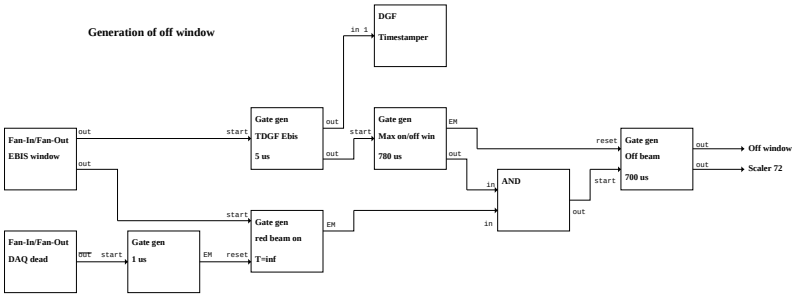

Figure 5: Generation of the off window

The off window is a window which starts after the DAQ readout has finished following the EBIS window. The idea is that we take data during the EBIS window, then read out that data and then acquire again after the EBIS gate has closed. It is the off window which defines the period of acquisition after the EBIS gate has closed.

Note that the TDGFEbis gate generator is irrelevant in the generation of the off window because the max on/off window triggers on its leading edge, so it could just as well have triggered on the EBIS window signal itself. However, the TDGF Ebis signal is also sent to the timestamping DGF, so it is needed and there are no free outputs left on the fan-in/fan-out of the EBIS window.

The max on/off window is 80 μs longer than the EBIS window and starts at the same time. The assumption is that we do **not** fill the DGF buffers during the EBIS window so readout only occurs at the end of the 700 μs of the EBIS window. That causes the DAQ to go busy for a time and we wait for the time when it goes from busy to not busy, then wait 1 μs and reset the read beam on gate generator. That gate generator is set to infinite time, so it is only when the reset occurs that it sends the end marker which triggers the off window, provided the 780 μs of the max on/off window hasn't expired.

We could run into serious problems if the DGFs fill up enough before the end of the EBIS window that the readout and the 1 μs delay are over before the end of the EBIS window, as this would result in the off window opening before the end of the EBIS window. That would cause in-beam events to end up in the off-beam window. At the moment, that shouldn't happen, simply because we don't expect to get that many DGF events in the EBIS window that a DGF buffer would fill up. However, we must not forget this if we add new systems to the acquisition! Note that this is not an issue for anything gated with the on/off pulse since such signals don't start until the beginning of the EBIS pulse and as readout takes longer than an EBIS pulse, even if the corresponding DGF were full at once, it could not cause this error. However, if a channel is free running, so that it starts at the end of the readout after the off window, it could conceivably be full enough **before** the EBIS pulse for readout to occur and finish during the EBIS pulse.

7 Generation of the on/off window

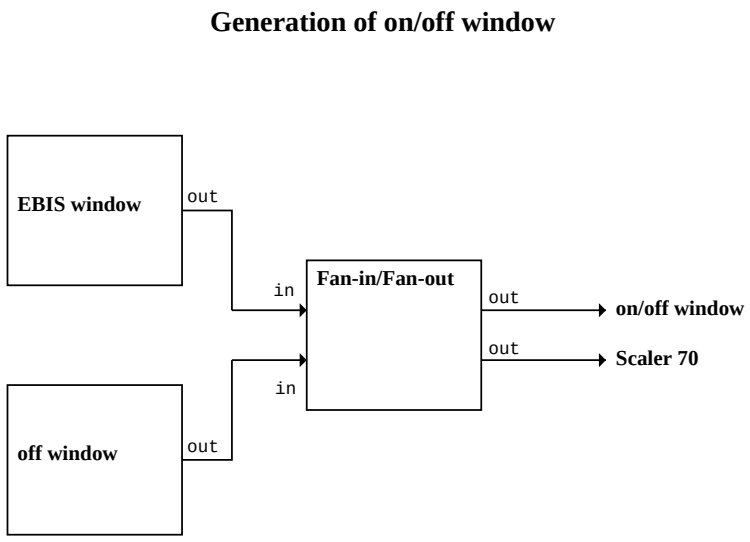

Figure 6: Generation of the on/off window (GFLT)

The on/off window is simply the logical OR of the EBIS window and the off window. It is equivalent to the GFLT which gates all the Miniball clusters and is also used to gate the main Si trigger to generate the DiscrNoBu signal.

8 The generation of the GFLT

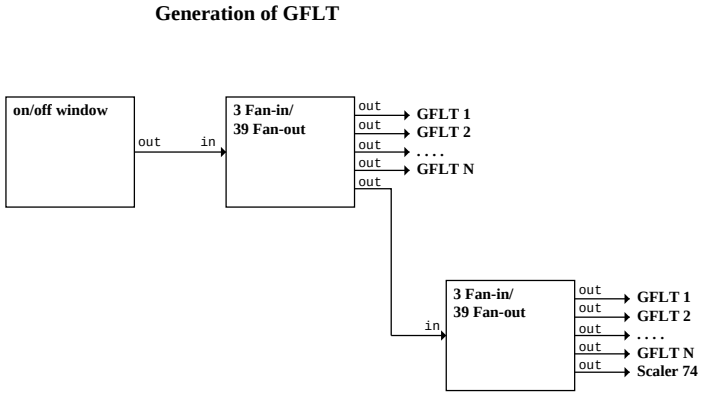

Figure 7: The generation of the GFLT from the on/off window

The global first level trigger (GFLT) signal which is sent to each DGF is essentially the on/off window.

9 Generation of forced readout

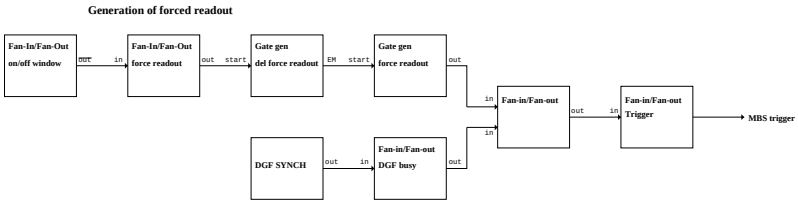

Figure 8: Generation of the forced readout

As soon as the on/off window closes, a DGF busy is generated to force a readout. This is fanned out to all the SYNCH inputs of the DGFs and also used to generate a DAQ trigger. Note that the trigger generated here is not actually sent to the MBS. It is the old trigger which was previously used. It is not actually necessary to perform a logical OR between the signal sent to the DGF BUSY input and the signal received from the DGF SYNCH output because the SYNCH is already the logical OR of the BUSY.

10 Generation of the pattern unit control signal

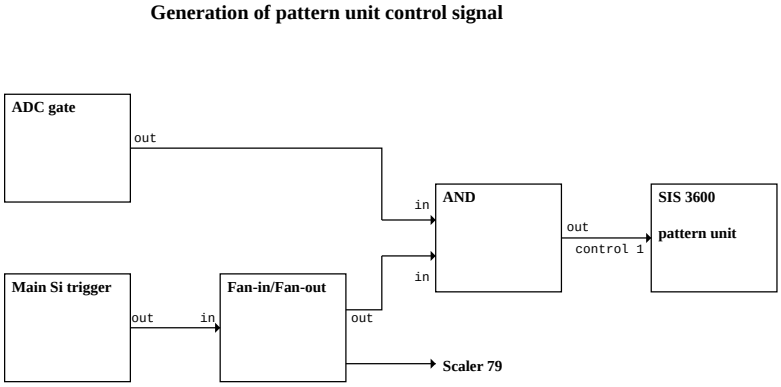

Figure 9: Generation of the control signal for the pattern unit

The SIS3600 pattern unit needs a control signal to tell it when to latch the bits of the pattern and add them to the data stream. This is generated by the logical AND of the main Si trigger and the ADC gate. Note that the only reason for the Fan-in/Fan-out unit is to provide an extra output for the scaler.

11 Generation of the control signals for the scalers

Like the SIS3600 pattern unit, the SIS38xx scalers require a control signal. This is generated by a 1 Hz clock signal after the EBIS pulse. Note that the OR seems to be completely superfluous.

12 Generation of the DGF scalers

The Mult Out of each DGF is sent into a TFA modified specially for Miniball by George Pascovici (it contains eight of George's preamps inside!). It converts the 35 mV per channel to a logic signal which is discriminated and sent to a scaler. Another copy of the signal is sent to a NIM to ECL convertor and then via flat cable to the TDC stop (channels 9 to 16). The OR output of the discriminator is also used to generate a trigger source for the GSI trigger box.

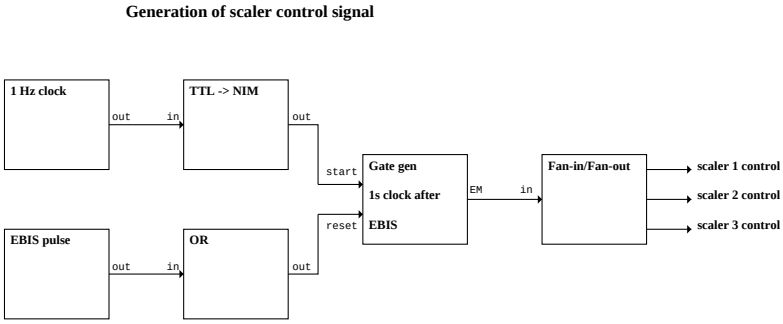

Figure 10: Generation of the control signals for the scalers

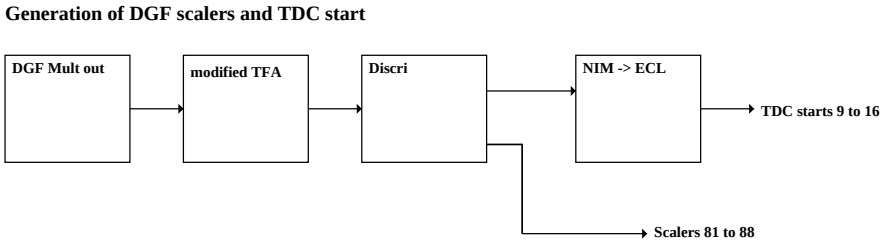

Figure 11: Generation of the scalers for each DGF

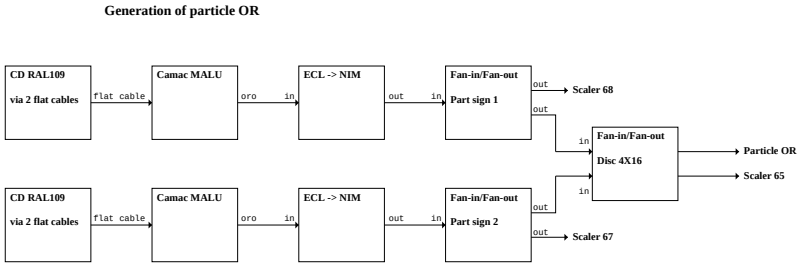

Figure 12: Generation of the particle OR

13 Generation of the particle OR

Each of the eight channels of the first eight RAL109 amplifiers from the CD electronics generates a logical signal (ECL) if a particle is detected. The signals

from pairs of modules are combined on four 16-wire flat cables and sent to two camac majority logic units (MALU), each of which provides a single ECL output (a simple OR of the inputs) which after conversion to NIM are again ORed together.

14 The DGF BUSY/SYNCH loop

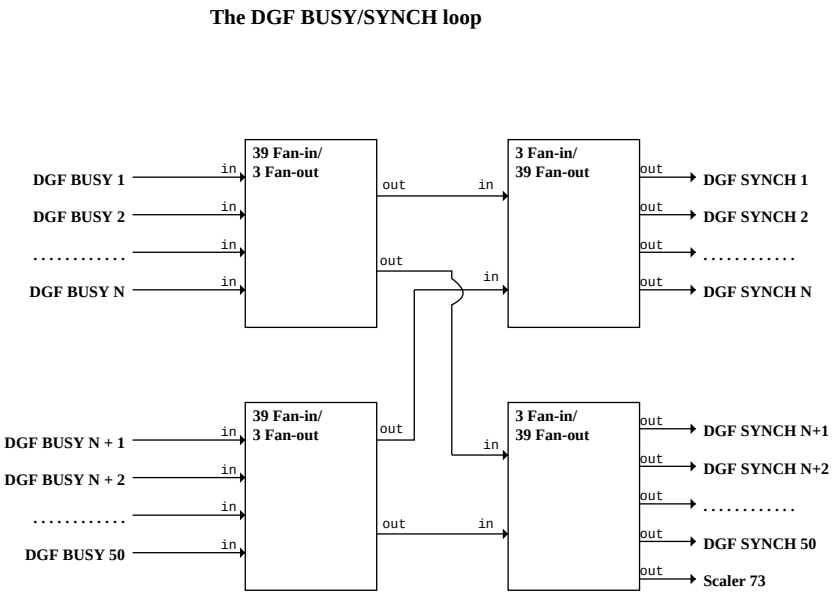

Figure 13: DGF BUSY/SYNCH loop

The DGF BUSY/SYNCH loop is made from two 39-Fan-in/3-Fan-Out modules and two 3-Fan-in/39-Fan-Out modules. We take the BUSY output from each DGF and feed it into the Fan-In inputs. We also take a signal which is used to force readout and feed it into the Fan-In. Furthermore, we take the DAQ dead signal and put it into the Fan-In to ensure that nothing can start until the DAQ has finished reading out. The outputs from each of the two Fan-In modules are sent to each of the Fan-Out modules, so that each Fan-Out modules give 39 output signals which are the logical OR of all the BUSY inputs and the forced readout. That signal is sent to each of the DGF SYNCH inputs and also used to start the DAQ trigger.

15 The generation of the trigger box inputs

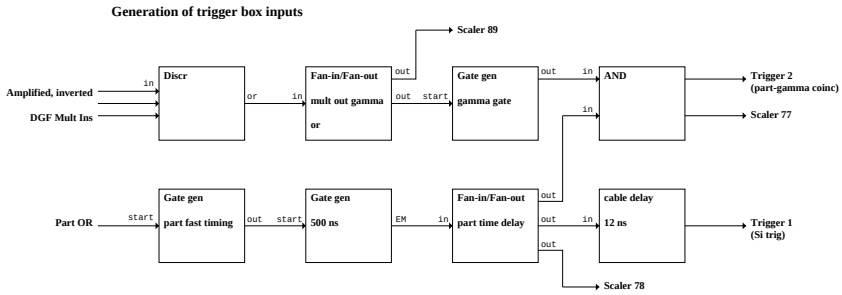

Figure 14: The generation of the inputs for the GSI trigger box

We generate two trigger sources for the GSI trigger box. The first is the logical AND of the particle OR and the DGF gamma trigger (derived from the Mult Out for each cluster, which is converted to NIM using the specially modified TFA and a discriminator. The other trigger source comes directly from the particle OR. The trigger box can then select one trigger or the other and perform any necessary downscaling.

Note that there are two gate generators in the particle OR branch, the first of which seems to be superfluous because the second one triggers off its leading edge. There seems to be no obvious reason for this.

16 The generation of the TDC starts and pattern unit bits

For the TDC, we use channels 3 for the PPAC, 7 for the particle-gamma coincidences, 8 for the downscaled particles and 9 to 16 for the DGF Mult Outs (per cluster trigger).

For the pattern unit we use channel 1 for the laser on/off, channel 2 for the downscaled particles and channel 3 for the particle-γ coincidences.

17 The generation of the T1 and BUSY signals

We gate the T1 signal (a TTL pulse sent to us when the protons are incident on the ISOLDE target) with the DGF SYNCH signal to generate T1 and BUSY and with the inverted DGF SYNCH signal to generate T1 and NOT BUSY.

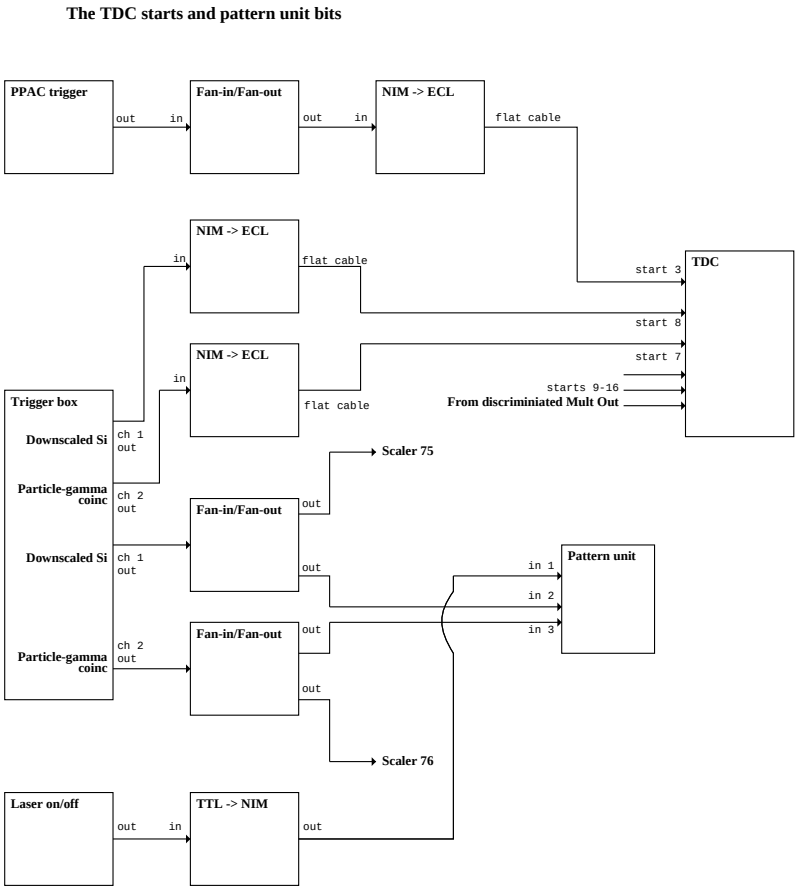

Figure 15: The generation of the TDC starts

18 The generation of the T1 spectrum

We generate a spectrum based on the T1 signal, so that each T1 pulse is counted in one of two peaks. We do this by taking T1 gated with BUSY and T1 gated with NOT BUSY, attenunate the former and sum the signals in a linear fan out. The result is an output which comes whenever a T1 pulse arrives with an amplitude which is high for busy and low for not busy. The DGF acquires a spectrum of this signal (i.e. two peaks).

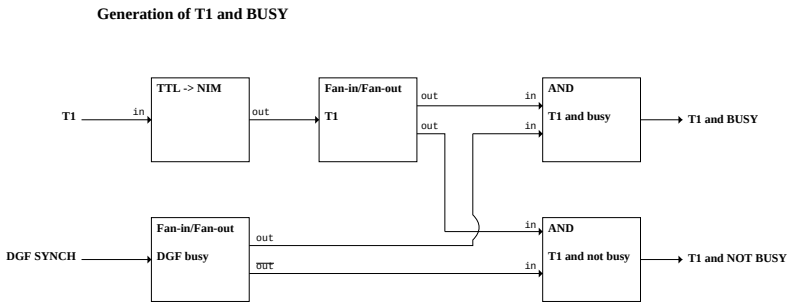

Figure 16: The generation of the T1 and BUSY and the T1 and NOT BUSY signals

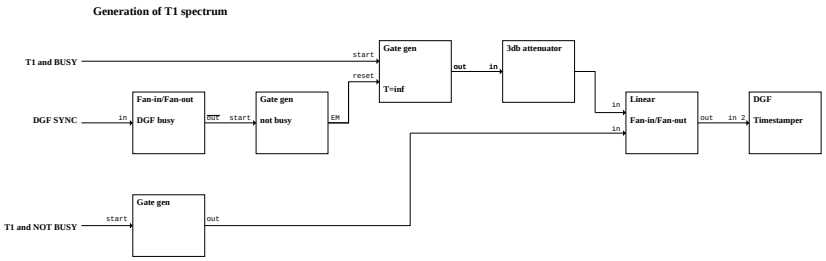

Figure 17: The generation of a spectrum with one peak for T1 and busy and one peak for T1 and NOT busy

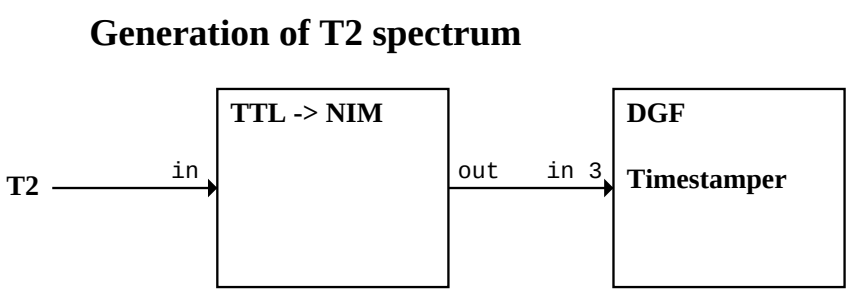

Figure 18: The generation of the T2 spectrum

19 The generation of the T2 spectrum

Note that the end of the T2 signal in the control room was not connected during this experiment, but it was cabled as shown.

20 The generation of the on/off window and 1 MHz signal

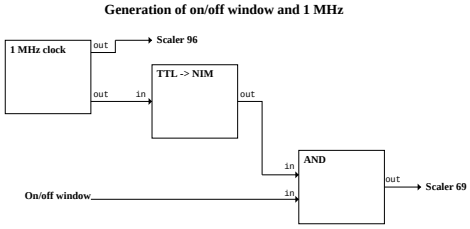

Figure 19: The generation of the 1 MHz signal gated by the on/off window

The 1 MHz pulse is used as a reference to normalise the other scalers and the gated 1 MHz gives the fraction of time that the system is live.

21 Scalers

There are three 32-channel scaler modules in use. Scalers 1 to 64 are for the PPAC. The third has a variety of different signals from different sources.

Scaler	Signal	Scaler	Signal
65	Si trig (free)	73	DGF SYNCH
66	Si trig (accepted)[1]	74	DGF GFLT
67	Si trig1	75	Downscaled Si trigger
68	Si trig2	76	Downscaled particle-γ coinc
69	on/off win AND 1 MHz	77	Particle-γ coinc
70	on/off window	78	Delayed Si trig
71	EBIS pulse	79	Total Si trig (free)
72	Off beam	80	X

Scaler	Signal	Scaler	Signal
81	Cluster 1	89	Total DGF
82	Cluster 2	90	X
83	Cluster 3	91	X
84	Cluster 4	92	X
85	Cluster 5	93	X
86	Cluster 6	94	Beam dump counter[1]
87	Cluster 7	95	Start detector[1]
88	Cluster 8	96	1 MHz clock

[1] Not connected.