Miniball electronics for Orsay

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1 Foreword

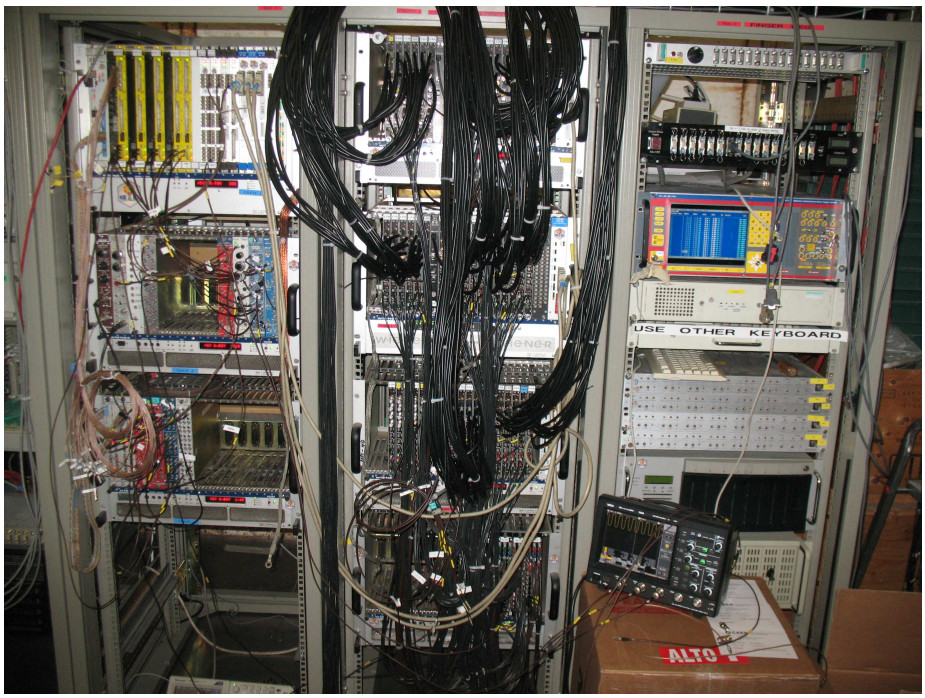

Figure 1: Racks 3, 4 and 5. We do not use the first rack at Orsay and in the second rack, we only have the DAQ computer and the PT100 readout. In rack 5, we only use the preamp power and HV mainframe.

The convention for naming slots is something like R3.C2.S9 which means rack 3 (counting from 1 on the far left to 5 on the far right), crate 2 (counting from 1 at the top, downwards) and slot 9 (as labelled on the crate - note that for NIM crates, modules occupy two slots, but we normally only give the first one).

This documentation corresponds to the state of the setup on 1st May 2014, when the setup was still a work in progress.

I recommend also referring to the last documentation for the Miniball electronics at CERN from April 2012 to see how we did things there.

2 Overview

The logic for the Miniball electronics and DAQ is set for in-beam spectroscopy studies with stable beams. The data should be read continuously so the trigger (GFLT and MADC gates) should limit the number of read events in order to

avoid the DAQ to be permanently in dead time. This means that we should determine, depending on the experiment, what type of coincidences is needed to optimize the data readout. As far as the accepted experiments are concerned these should be the following configurations:

- 2 or 3 fold gamma coincidences. This will be done using the MultOut of the DGFs and a LED for positif signals.
- gamma AND particle. Particle can be either the plastic detector at forward angles, or the annular detector at backward angles.
- delayed 3 fold gamma coincidence. This is for the LICORNE experiment.

We only intend to use to code the detector signals:

- DGF for the Miniball and ORGAM detectors.
- MADCs for the particle detectors and for the AC BGO shields.

Additional control signals might be added on the MADC or DGF. For the moment, we don't intent to use the BitPattern module, but this might change.

This documentation corresponds to the state of the setup on 1st June 2014. Still the setup might change.

I recommend also referring to the last documentation for the Miniball electronics at CERN from April 2012 to see how we did things there.

3 The DGF BUSY/SYNCH loop

The DGF BUSY/SYNCH loop is made using two 39-fan-in/3-fan-out modules and two 3-fan-in/39-fan-out modules. We take all the BUSY outputs from the DGFs and feed them into the fan-in inputs and then take the outputs to the fan-outs and send the result to each SYNCH input. In this way, if any one DGF is BUSY, the SYNCH line is set to logic one and if all the DGFs are acquiring it is logic zero.

The BUSY/SYNCH loop serves three purposes:

- At the start of a run, a bit is set in the DGF, which tells it to zero its clock when the SYNCH goes from logic 1 to logic 0. This happens, when the last DGF drops its BUSY.
- When a DGF has a full buffer, it sets its BUSY. This tells all the other DGFs to terminate their buffers.
- When a DGF has a full buffer, the SYNCH signal goes from logic 0 to logic 1 and this is used to trigger the DAQ readout.

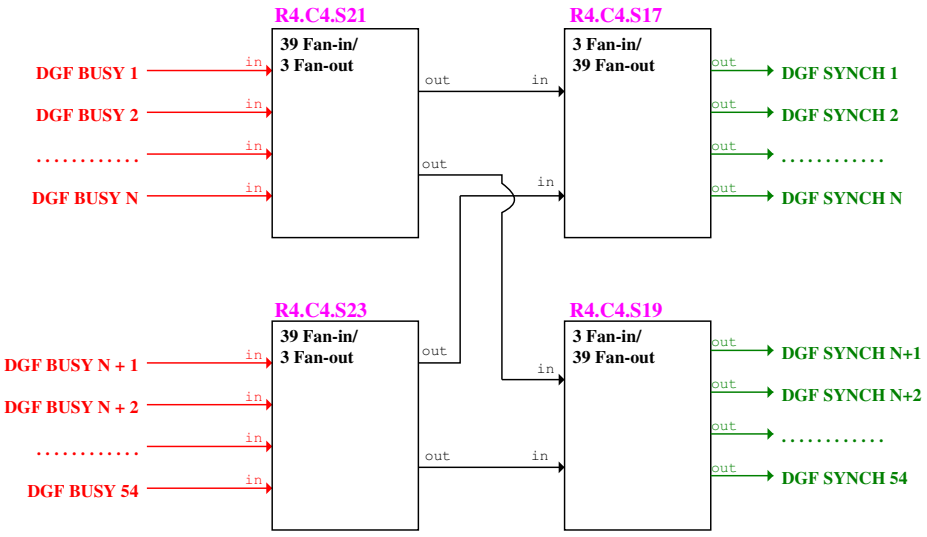

Figure 2: The DGF BUSY/SYNCH loop. This is used to synchronize the DGFs and trigger the DAQ readout.

- BUSY (DGF output) - is at 0 when DGFs are free to acquire data. Is at 1 when a DGF has a full buffer.
- SYNC (DGF input) - whenever one of the BUSY signals from DGF goes to 1, then the SYNC goes to 1 and is send to all of the DGFs.
-

4 The GFLT fan-out

The global first level trigger (GFLT) signal which is sent to each DGF determines whether an event is validated or not. It needs to be sent after the slow filter of the DGF. Starting from the Mult Out signal, we wait **SLOWLENGTH + SLOWGAP + 400 ns**, where SLOWLENGTH and SLOWGAP are DGF parameters (normally 6800 and 1200 ns, respectively - note that the actual parameter is the time divided by 400 ns), then open the gate for **800 ns**. This is completely different to the operation at ISOLDE, where we open the GFLT for the length of the beam pulse and then a second time off beam.

GFLT starts 8.4 μs after Mult Out signal and lasts 800 ns

The GFLT will have to be adapted to each experiment at Orsay. It might be one of the following:

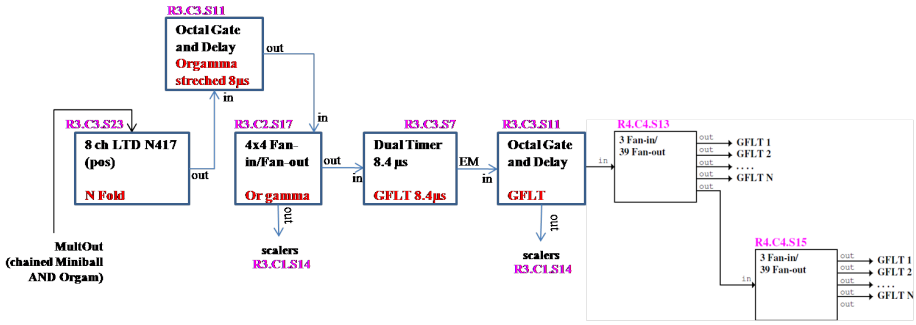

Figure 3: The fan-out of the GFLT, set up for singles. The triple AND unit has no input on it and we use the inverted output to generate a continuous NIM logic 1.

- Constant logic 1 - i.e. singles
- γ-γ coincidences
- particle-γ coincidences

We use two 3 fan-in 39 fan-out modules to distribute the signal to all the DGF modules.

5 The DAQ dead and DAQ go

The VME trigger module (that triggers the readout of the buffers stored in the DGFs and MADCs) provides 2 signals:

- DAQdead : this signal is sent on ECL out, pins 7 and 8 (pins should be counted from bottom to top). Is set on logic 1 when a DAQtrig signal is send to the input of the trigger module. Goes to 0 when the data read out is finished.
- DAQgo : this signal is on ECL out, pins 9 and 10. Is at logic 1 when the acquisition is stopped. It goes to 0 after a StartAcq and stays as long as the acq is running. Used to reset the clock of MADCs.

6 Generation of the DAQ dead signals

There are two signals:

- DAQ dead, which is a NIM version of the signal generated by the DAQ trigger

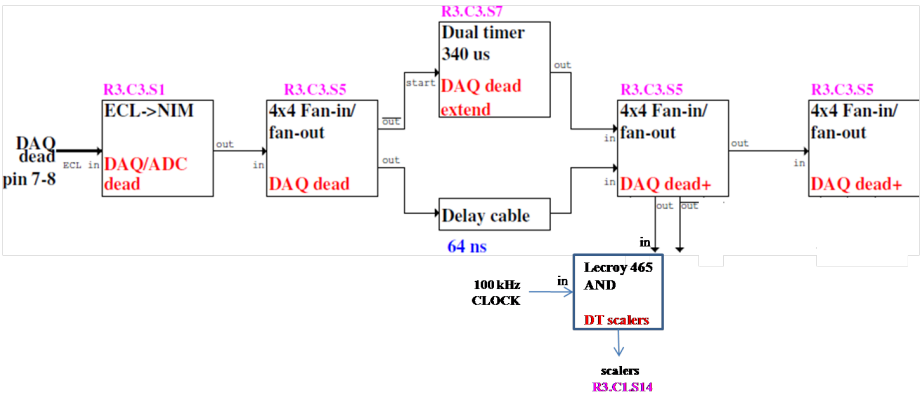

Figure 4: The generation DAQ dead signals. The main "DAQ dead" signal is just a NIM version of the signal from the VME trigger module. The "DAQ dead+" is the same thing extended by 340 μs.

- DAQ dead+, which is the same thing extended by 340 μs.

The VME trigger module has an ECL output indicating that the DAQ is dead on pins 7-8 (note that pins 1-2 are the lower ones and 15-16 the upper ones). This goes through an ECL to NIM converter, after which it is split into two. One part is delayed by a 64 ns cable and the other part is used to start a gate at the end of the DAQ dead time. The idea is to extend the DAQ dead produced by the VME trigger by a fixed amount. If we were to do this without the delay, we might get a short glitch where it goes not dead between the end of the output from the VME trigger module and the beginning of the extension. After that it is fanned out.

The DAQ dead extend was set to 340 μs.

7 Generation of the DAQ trigger signal

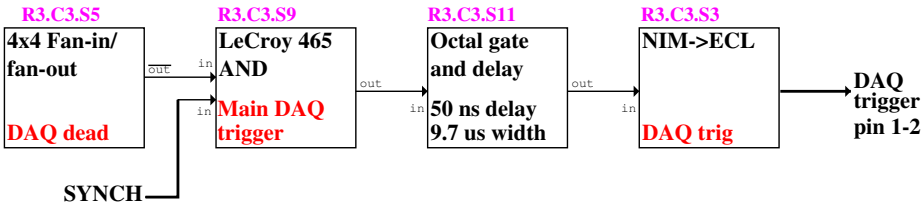

Figure 5: The generation DAQ trigger signal.

The DAQ trigger is generated by the "SYNCH" signal, which is the OR of all the BUSY signals of all the DGFs. When the first DGF has a full buffer, it sets

its BUSY and the SYNCH goes from logic 0 to logic 1. This is used to start a gate, but only if the DAQ is not dead. The delay is set to its minimum and the length is a little under 10 μs. This is converted from NIM to ECL and sent to the input of the VME trigger (R3.C1.S2).

8 The MADC32 40 MHz clock

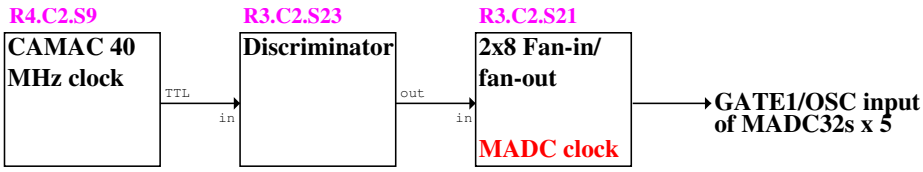

Figure 6: The generation of the 40 MHz clock signal for the MADC. One clock signal goes to each of the five MADC32s. Normally, we use a TTL $\rightarrow$ NIM instead of the discriminator. This version is a workaround due to a broken clock module.

Like the DGFs, the MADC32s use a 40 MHz clock for timestamping. In fact, they use the same 40 MHz signal.

Normally, each of the three CAMAC 40 MHz clock modules (one per CAMAC crate) can generate a TTL version of the signal and we use a TTL $\rightarrow$ NIM converter to convert it to NIM and then fan it out. However, the clock modules in the first and third CAMAC crates are completely broken and give no TTL output and the one in the second crate gives an attenuated output. So a TTL $\rightarrow$ NIM converter doesn't work. This is not normal. Something is broken.

The workaround is to replace the TTL $\rightarrow$ NIM with a LeCroy 821 quad discriminator and use one of its four channels to discriminate the signal and convert it to NIM. This seems to work.

9 The MADC32 reset clock

Like the DGFs, the MADC32s, the MADC32s have to reset their clocks at the beginning of each run. However, while the DGF has a software bit to tell it whether to reset the clock when the SYNCH goes from logic 1 to logic 0, the MADC32s have a reset input. So we use an additional signal from the DAQ called "DAQ go", which is generated at the beginning of each run (but not on each buffer). It comes from pins 9 and 10 of the VME trigger module and is converted to NIM and used to start a timer. This timer is stopped by the inverted SYNCH output. i.e. when the run starts, we start the timer, then we stop it when the last DGF drops its busy. The end marker from this timer is

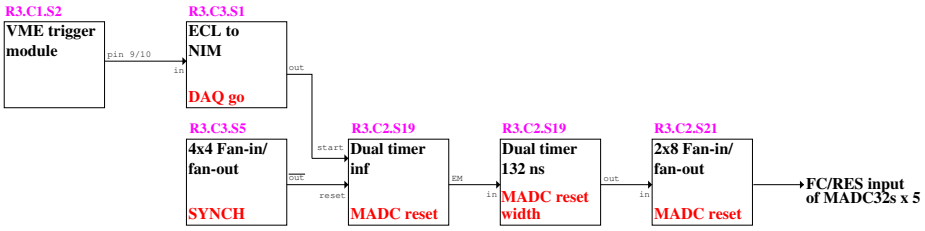

Figure 7: The generation of the MADC32 reset from the DAQ go and DGF SYNCH signals

used to start a second timer, which provides a 132 ns pulse, that is fanned out to the reset inputs of the five MADCs.

10 The generation of the MADC32 gates

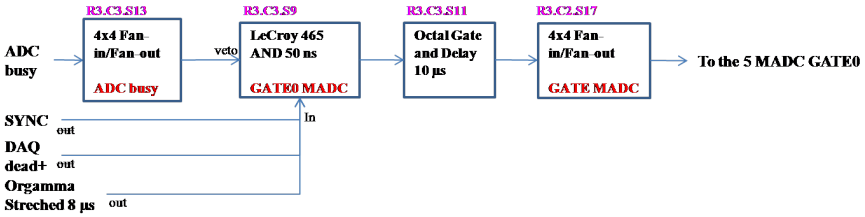

Figure 8: The generation of the MADC32 GATE0

We need to apply a gate to each MADC32 in order to make it read out. However, we should not send gates if:

- The DAQ is dead (in fact we use the "DAQ dead+" signal for this).
- The DGFs are dead (i.e. the "SYNCH" signal).
- The ADC itself is dead (it has a busy output) and we might want to combine the dead signals from the five MADC32s in case we want common dead time.

11 The scaler control signal

Every second, we send a pulse to the control input of each of the three VME scalers. This causes the DAQ to read them out. It also triggers readout of the DGF scalers.

At the moment we are not making use of the scalers, but they are an important diagnostic tool.

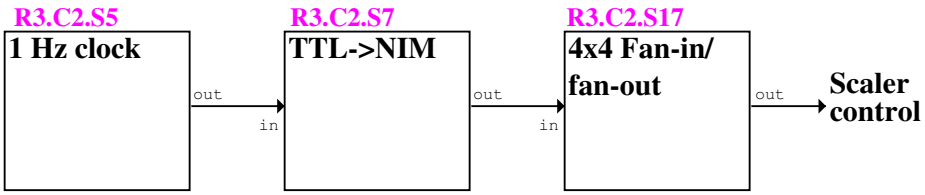

Figure 9: The generation of the scaler control signal

12 The pattern unit control signal

So far, we haven't cabled this up. If a pulse is sent to the control input of the pattern unit, it will latch the current logic states of its 32 inputs and store that in the data stream.

However, we need to be careful that we can, later on, identify which pattern occured when. Unfortunately, the pattern unit has no timestamping.

13 DGF backplane bus

The DGFs need to have a common 40 MHz clock shared by all modules, which is connected via the backplane bus. This is generated by one of the CAMAC 40 MHz clock modules, which is set to master. Never connect an input to a module set to master. The output of the master goes to the input of another clock set to slave and its output goes to the input of a third module set to slave etc. These connections are made with IEEE-1394 (Firewire) cables at the front.

At the back of these clock modules there are three outputs which can be used to fan out to up to eight DGFs per output. So one module is enough per crate. A flat cable is used to connect each DGF to the clock with an adaptor piece at one end and a terminator piece at the other.

The DGF has two triggers: a fast trigger sent as soon as an event is detected and a slow DSP trigger sent after the slow filter time (i.e. about 10 μs later. These are available on the same backplane bus as the 40 MHz clock. For Miniball, we have seven signals per capsule on two DGFs, and only the core is allowed to generate a signal. So the trigger lines between those two DGFs need to be connected. Then the core channel can trigger the segments in the same DGF and those in the second DGF. The trigger lines between DGF modules with signals from different clusters should be cut. To do this, physically cut out the four middle wires of the 16 wire flat cable between modules that are not for the same capsule, but leave the other wires (clock etc.) present. Note, that for the special signals for the timestamping DGFs, these are all independent, so all the trigger wires should be cut there.

Unfortunately, because the DGF bus is incorrectly terminated, it was not possible to protect the driver IC of the clock module against misconnection. So if you connect up something wrongly, you will probably blow the AD8017 driver IC for that channel. Don't then swap the channels or you will kill another one!

14 Positions of modules in crates and racks

The racks are numbered from 1 to 5 with 1 being closest to the wall. The crates are numbered from 1 with crate 1 being highest. The notation R1.C2 means rack one crate two and R1.C2.S17 refers to the module in slot 17 of that crate. These numbers are shown on the circuit diagrams.

14.1 Rack 1

This rack has various crates which are not used.

14.2 Rack 2

This rack has the CD electronics (unused), the PT100 readout and the DAQ computer.

14.3 Rack 3

In rack 3 we have a VME crate and two high-power NIM crates.

14.3.1 VME crate R3.C1 for Coulex

- Slot 1 - power PC
- Slot 2 - VME trigger module
- Slot 3 - empty
- Slot 4 - Mesytec MADC32 0x00F10000
- Slot 5 - empty
- Slot 6 - Mesytec MADC32 0x00F30000
- Slot 7 - empty
- Slot 8 - Mesytec MADC32 0x00F40000
- Slot 9 - empty
- Slot 10 - Mesytec MADC32 0x00F50000
- Slot 11 - Mesytec MADC32 0x00F60000

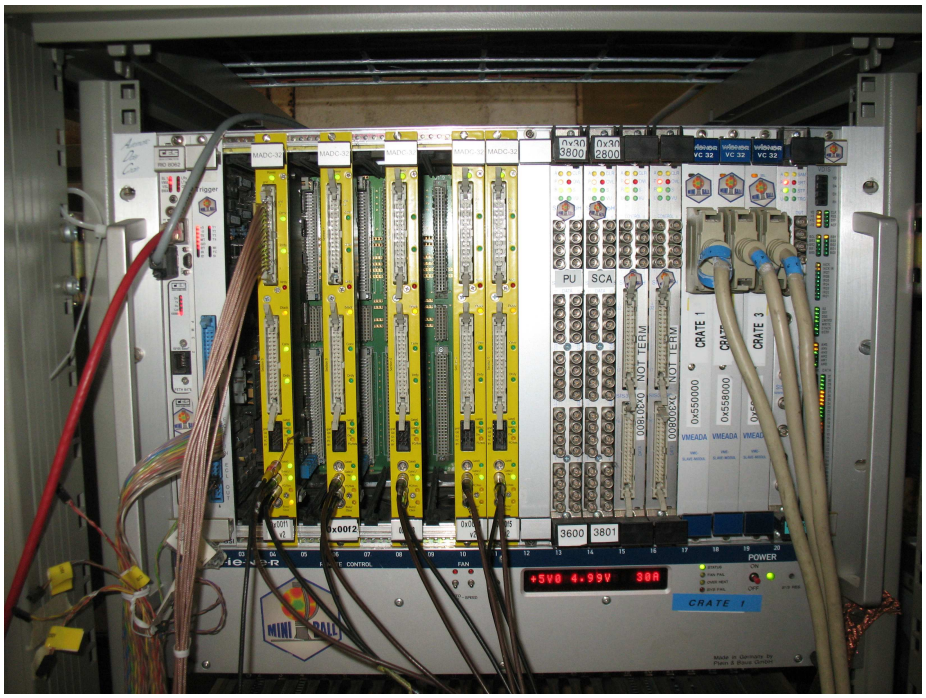

Figure 10: R3.C1: power PC, VME trigger module, five MADCs, pattern unit, three scalers (one with LEMO inputs, two with flat cable) and the VC32 modules with the SCSI cables going to the CAMAC crates.

- Slot 12 - blank
- Slot 13 - pattern unit 0x00303800
- Slot 14 - scaler with NIM inputs 0x00302800
- Slot 15 - scaler with ECL inputs (PPAC X) 0x00300800
- Slot 16 - scaler with ECL inputs (PPAC Y) 0x00301800
- Slot 17 - Wiener VC32 (CAMAC 1) 0x00550000
- Slot 18 - Wiener VC32 (CAMAC 2) 0x00558000
- Slot 19 - Wiener VC32 (CAMAC 3) 0x00560000
- Slot 20 - SiS 3300 100 MHz 12 bit ADC (Bragg Detector) 0x40000000
- Slot 21 - VDIS

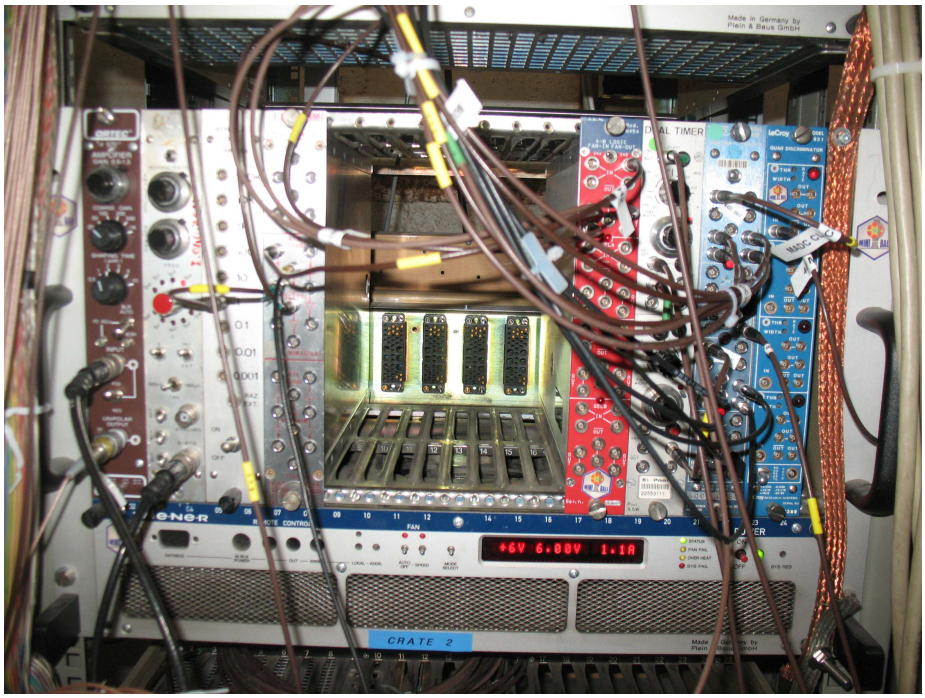

Figure 11: R3.C2

14.3.2 NIM crate R3.C2

- Slot 1-2 - Ortec 570 amplifier
- Slot 3-4 - empty
- Slot 5-6 - No-name clock : 100 kHz for dead time measurements, 1 Hz for scaler readout
- Slot 7-8 - HMI level adapter : used with the No-name clock
- Slot 9-16 - empty
- Slot 17-18 - Caen N454 4x4 fan-in/out: 1 Hz scaler readout, Gate0 MADC, Gate0 MADC, ORgamma

- Slot 19-20 - No-name dual timer: DAQ go until synch, DAQ trigger for MADC reset
- Slot 21-22 - LeCroy 429 2x8 fan-in/out: MADC clock, MADC reset
- Slot 23-24 - LeCroy 821 quad discriminator: 40 MHz, unused, unused, 100kHz clock

14.3.3 NIM crate R3.C3

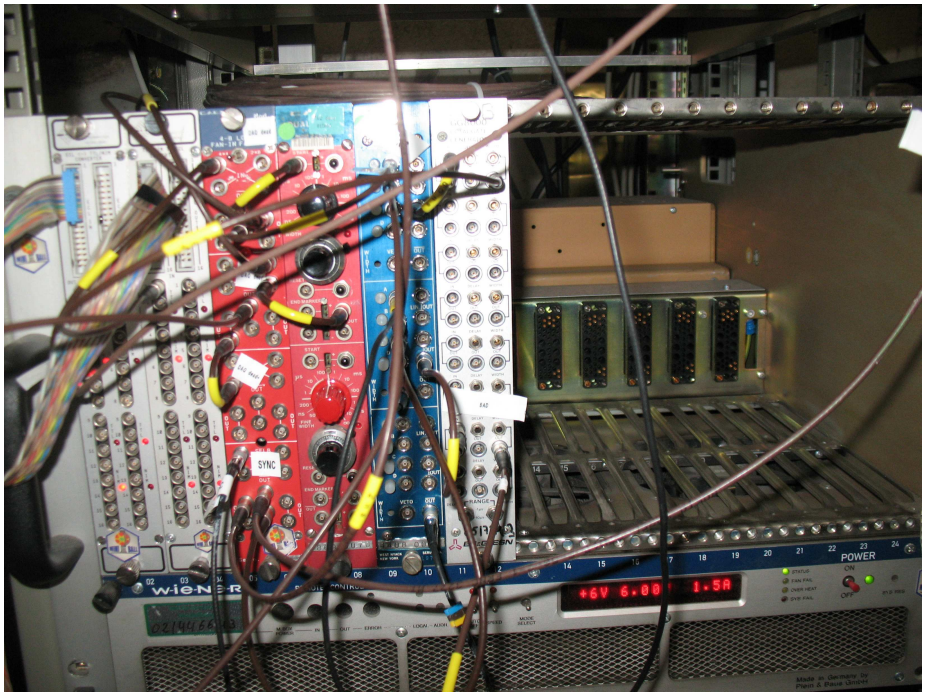

Figure 12: R3.C3

- Slot 1-2 - ECL to NIM converter
- Slot 3-4 - NIM to ECL converter
- Slot 5-6 - Caen 4x4 fan-in/out: daq dead, daq dead+, daq dead+, synch

- Slot 7-8 - Caen dual timer: daq dead extend, GFLT 8.4?s
- Slot 9-10 - LeCroy 465 triple AND: daq trigger, madc gate, Daq dead+ AND 100kHz for scalers
- Slot 11-12 - GG8000 octal gate and delay: daq trigger, unused, unused, ORpart gate, ORgamma width 8 ?s, bad, madc gate, GFLT 400 ns
- Slot 13-14 - LeCroy 429 2x8 fan-in/out: BUSY MADC, GFLT distribution
- Slot 15-16 - empty
- Slot 17-22 - TB8000
- Slot 23-24 - 8 ch Caen Low Threshold Discriminator N417: MultOut threshold, empty ...

14.3.4 NIM crate R3.C4

- Slot 1-2 - empty
- Slot 3-4 - STM 16 for BGOs
- Slot 5-6 - NIM/ECL/NIM convertor N638
- Slot 7-8 - STM 16 for 8 plastic detector
- Slot 9-18 - empty (one unused - yet - 16 ch Mesytec MSCF amplifier in 11-12)
- Slot 19-20 - LeCroy 370C Strobed Coincidence Unit: empty ...
- Slot 21-22 - LeCroy 429A 4x4 fan in/out: OR of all triggers, empty ...
- Slot 23-24 - LeCroy 365AL Four Fold Coincidence Unit: SYNC AND GFLT for scalers, ORgamma vetoed by particle bar

14.4 Rack 4

In rack 4 we have three CAMAC crates and one high-power NIM crate.

14.4.1 CAMAC crate R4.C1

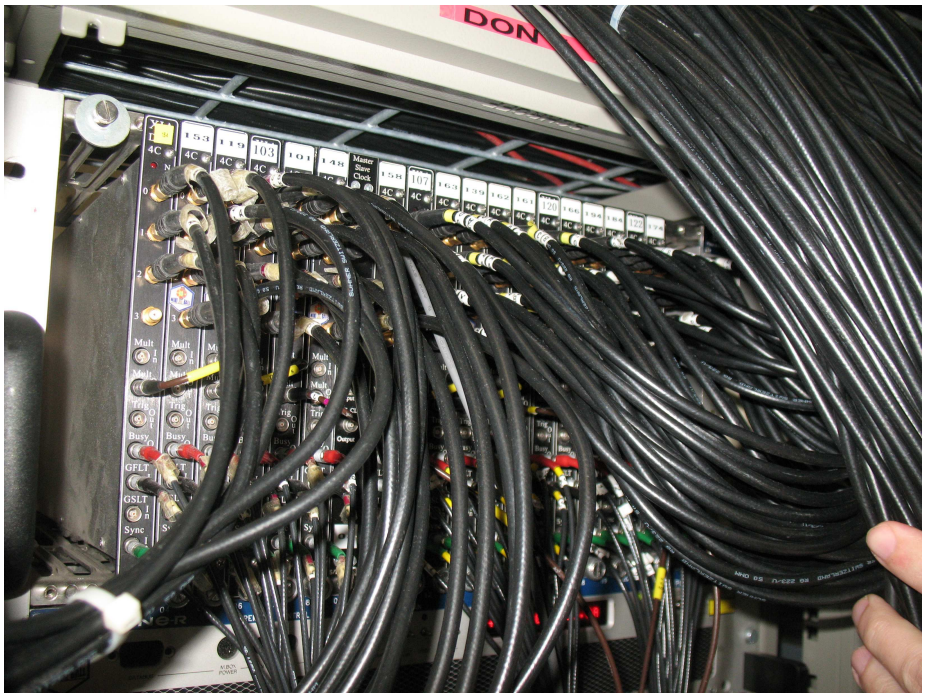

Figure 13: R4.C1

- Slot 3 - XIA DGF 1154
- Slot 4 - XIA DGF 1153
- Slot 5 - XIA DGF 1119
- Slot 6 - XIA DGF 1103
- Slot 7 - XIA DGF 1101
- Slot 8 - XIA DGF 1148
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1158
- Slot 11 - XIA DGF 1107

- Slot 12 - XIA DGF 1163
- Slot 13 - XIA DGF 1139
- Slot 14 - XIA DGF 1162
- Slot 15 - XIA DGF 1161
- Slot 16 - XIA DGF 1120
- Slot 17 - XIA DGF 1166
- Slot 18 - XIA DGF 1194
- Slot 19 - XIA DGF 1184
- Slot 20 - XIA DGF 1122
- Slot 21 - XIA DGF 1174
- Slot 24-25 Wiener CC32

14.4.2 CAMAC crate R4.C2

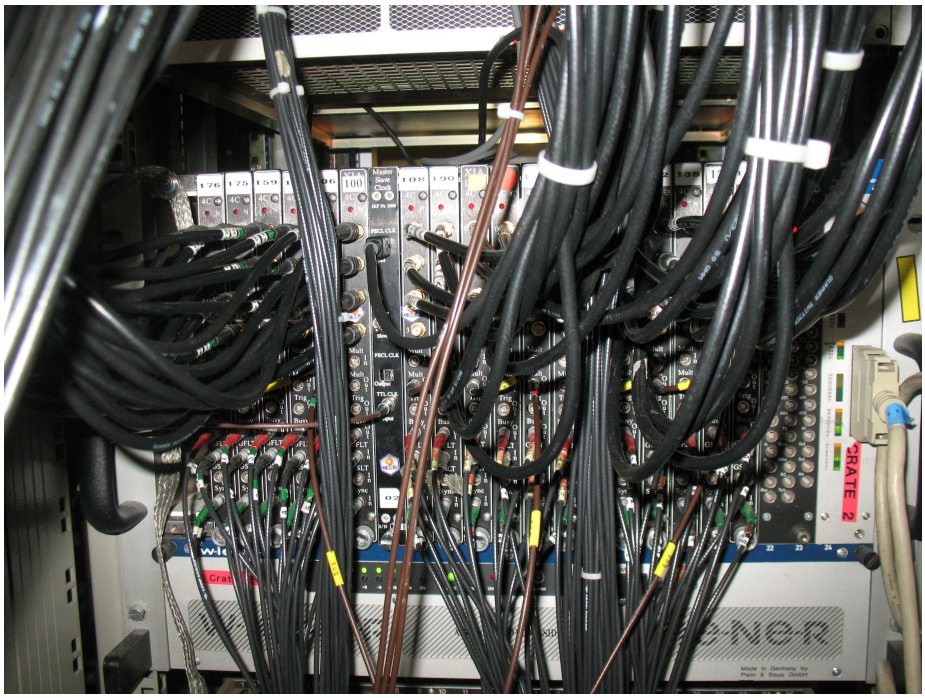

Figure 14: R4.C2

- Slot 3 - XIA DGF 1176
- Slot 4 - XIA DGF 1175
- Slot 5 - XIA DGF 1159
- Slot 6 - XIA DGF 1171
- Slot 7 - XIA DGF 1106
- Slot 8 - XIA DGF 1100
- Slot 9 - IKP 40 MHz clock
- Slot 10 - XIA DGF 1108
- Slot 11 - XIA DGF 1190
- Slot 12 - XIA DGF 1152
- Slot 13 - XIA DGF 1167
- Slot 14 - XIA DGF 1113
- Slot 15 - XIA DGF 1104
- Slot 16 - XIA DGF 1130
- Slot 17 - XIA DGF 1123
- Slot 18 - XIA DGF 1192
- Slot 19 - XIA DGF 1138
- Slot 20 - XIA DGF 1128
- Slot 21 - XIA DGF 1147
- Slots 22,23 - additional 40 MHz clock
- Slot 24-25 Wiener CC32

14.4.3 R4.C3

- Slot 4 - XIA DGF 1132
- Slot 5 - XIA DGF 1178
- Slot 6 - XIA DGF 1149
- Slot 7 - XIA DGF 1137
- Slot 8 - XIA DGF 1142
- Slot 9 - XIA DGF 1189

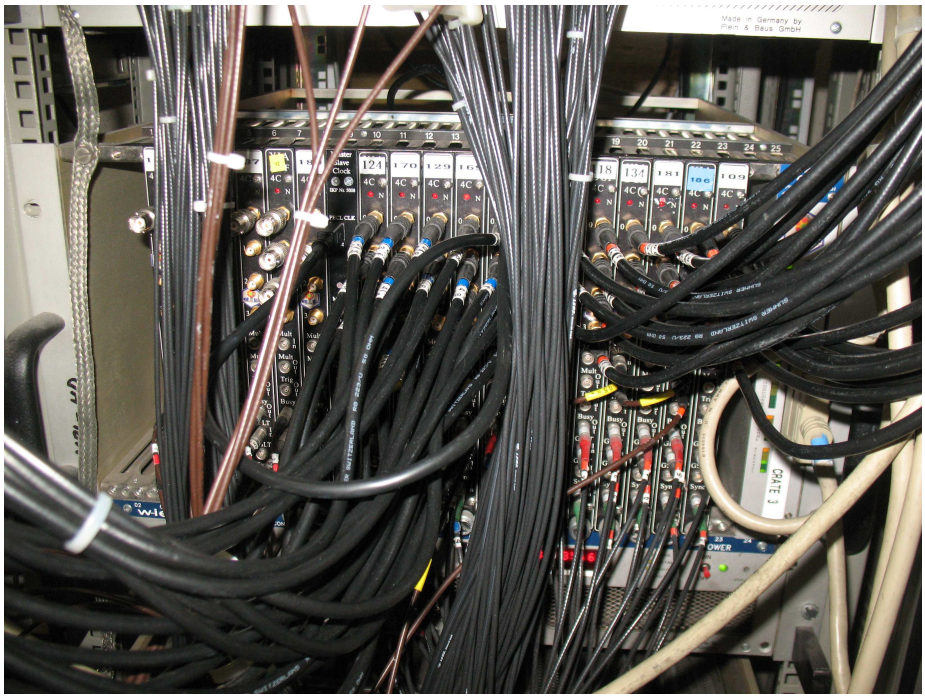

Figure 15: R4.C3

- Slot 10 - IKP 40 MHz clock
- Slot 11 - XIA DGF 1124
- Slot 12 - XIA DGF 1170
- Slot 13 - XIA DGF 1129
- Slot 14 - XIA DGF 1169
- Slot 15 - XIA DGF 1151
- Slot 16 - XIA DGF 1150
- Slot 17 - XIA DGF 1145
- Slot 18 - XIA DGF 1118
- Slot 19 - XIA DGF 1134
- Slot 20 - XIA DGF 1181
- Slot 21 - XIA DGF 1186
- Slot 22 - XIA DGF 1109
- Slot 24-25 Wiener CC32

14.4.4 NIM crate R4.C4

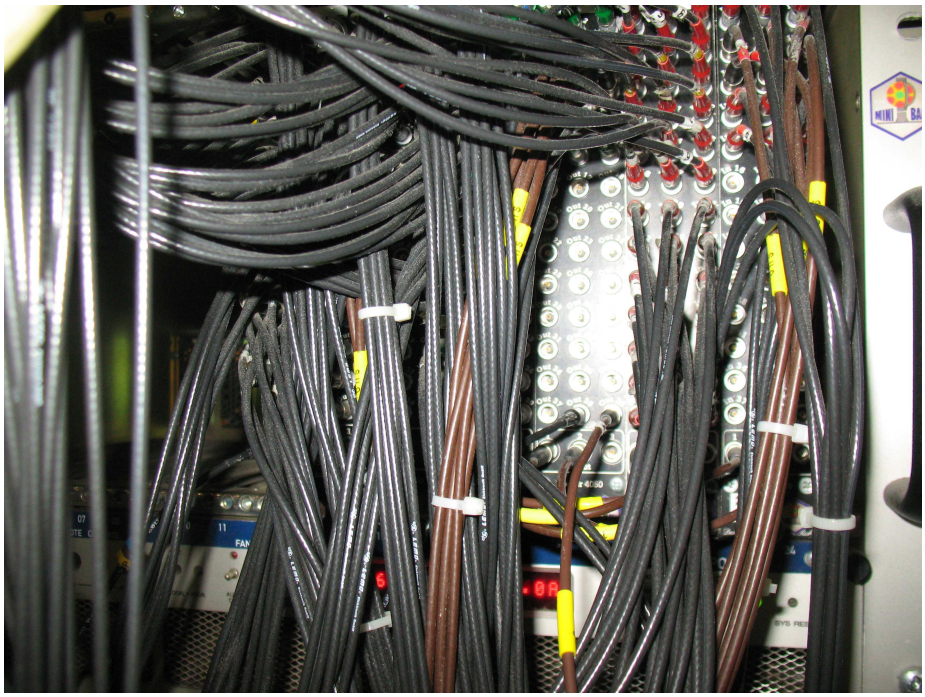

Figure 16: R4.C4 - This just has six fan-in/out modules. The first four have each 3 inputs and 39 outputs, while the rightmost two have 39 inputs and 3 outputs.

- 1-12 - empty
- 13-14 - IKP 3 fan-in/39 fan-out "GFLT"
- 15-16 - IKP 3 fan-in/39 fan-out "GFLT"
- 17-18 - IKP 3 fan-in/39 fan-out "Synch"
- 19-20 - IKP 3 fan-in/39 fan-out "Synch"
- 21-22 - IKP 39 fan-in/3 fan-out "Busy"
- 23-24 - IKP 39 fan-in/3 fan-out "Busy"

14.5 Rack 5

This rack has the old PT100 readout (unused), the preamp power, the HV mainframe, the old autofill computer (unused), the four manifold controllers

(unused), the old DAQ computer (unused), the old RAID array (unused) and the UPS (unused).

i.e. we only use the preamp power supply and HV mainframe.